Effects of TVS Integration on System Level ESD Robustness

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50 Words Abstract - Higher integration of Transient Voltage Suppression (TVS) functionality into ASIC I/O cells implies lower system costs. But as the ESD pulse is directed deeper into the system, migrating the TVS clamping function from the periphery of the system to a central ASIC may actually reduce the system's ESD robustness. ESD current reconstruction scanning can be used to trace the current path on a PCB, and possibly within an IC. The article compares the current spreading during and ESD for different ESD protection methods.

I. Introduction

The inevitable trend in system design for ESD robustness has tended toward higher integration of Transient Voltage Suppression (TVS) functionality into ASIC I/O cells. In low cost systems where the entire device has been distilled into a single "System on a Chip" (SOC) and perhaps an additional DDR memory device and a power supply and clock generator, the addition of discrete TVS devices near I/O connector ports can add appreciable costs to the parts count and in the case of a system with just a few USB or Ethernet ports, can double the assembly/placement costs for the entire PCB.

By shifting the ESD clamping into the highly integrated SOC these costs can be eliminated, however, this requires that the aggressor ESD pulse must be allowed to travel deep into the system where new susceptibilities to system upset may be triggered. While the cost is reduced, and the system ESD level survivability (resistance to permanent damage and hard failures) may be retained, the relocation of TVS clamping from the periphery of the system PCB to a central ASIC may actually reduce the system's ESD robustness and resistance to upset and soft errors.

This paper demonstrates an improved methodology for quantitatively analyzing and potentially predicting robustness of different system level ESD protection circuits, topologies and layout permutations on a given product. The methodology uses current reconstruction scanning, a methodology to observe the ESD current spreading in a time resolved fashion [2, 5, 6].

II. Measurement Techniques

The objective of this analysis is to characterize what happens throughout the PCB, at various "nearby" nodes when an ESD pulse enters the system through an I/O port, or other means.

Two different analysis techniques are used:

- Susceptibility scanning: This determines the local susceptibility of circuits to field injected noise, e.g. ESD like pulses
- Current reconstruction scanning: This determines in a time resolved fashion the spread of current after an ESD strike on the system

What is needed is an analysis technique to quantitatively identify all areas of susceptibility on a board, and then relate that to potential I/O entry vectors. This makes it possible for the designer to correlate and potentially predict how a system level IEC61000-4-2 ESD strike may cause a system upset, and provides a method for objectively comparing improvements to the system design.

For example, a designer with a prototype failing minimum system level ESD testing may need to compare different types of discrete TVS clamp solutions near the I/O connector, versus a cost-reduced alternative I/O cell integrated into an interior system ASIC.

It is a common practice to place ESD protection as close to the perimeter of the system as possible in order to shunt the energy back to the chassis and out of the system as soon as possible.

However, even in the case of a well protected system, upset in an apparently unrelated subsystem may still occur (i.e. an ESD strike to a USB port upsets a PC's video memory) making blind debug of the system upset extremely problematic.

By combining ESD susceptibility scanning [5] with a new reciprocal technique for "current spread" scanning [1,3,6], a matrix of potentially related aggressor and victim nodes can be identified and provide a comparative focal point for iterative improvement in design robustness.

A. Susceptibility Scanning Testing

1. Equipment

The scanning setup comprises a robotic 3D scanner with test control computer, Transmission Line Pulser (TLP), and DSO for data capture (See Figure 1).

We used the SmartScan system from Amber Precision Instruments [2]. For this test a 10mm horizontal loop probe was used for field injection (Figure 2). The maximum TLP charge level is set be a non-destructive 1kV, with a modified network to minimize the falling edge rate applied (Figure 2).

The scanning resolution is 5 by 5 mm and can traverse the entire system PCB area. When desirable, the system PCB can be mounted in as much of the system level enclosure as desired for closer relation to system level tests. The primary objective here is to probe the extent of the PCB design, routing and components, given a fixed case and mounting enclosure for the product. Certain systems, especially small handheld devices may dramatically hinder access to stacked PCBs or grounding brackets and consideration should be given to the extents of the scans.

Figure 1: Loop Probe with 10mm diameter

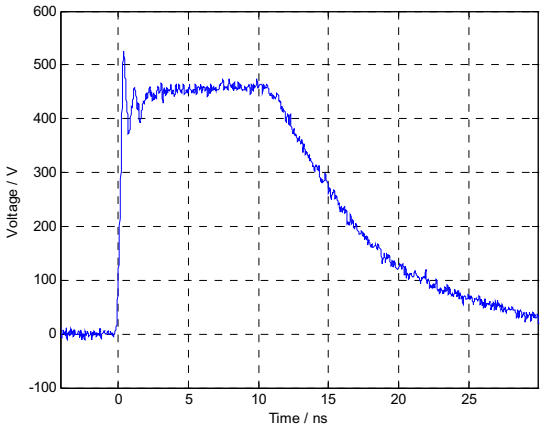


Figure 2: Injected modified TLP waveform into 50 ohm load

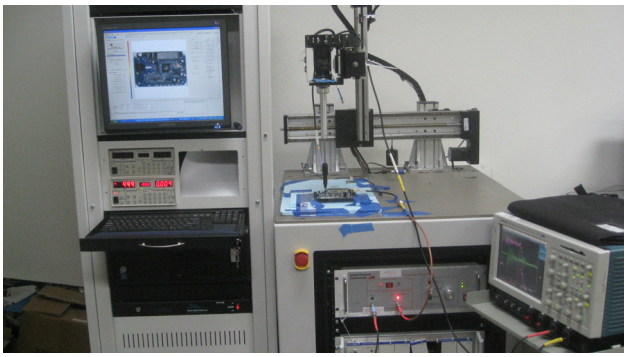


Figure 3: Photo of Scanning System

2. Procedure

The iterative scanning process traverses a predetermined area of interest on the PCB, alternately injecting a pulse, and then checking the system under test for continued operation. The initial pulse is 4kV until a system upset is detected and the stepped failure level is then tested at the failure location and recorded. In this particular example, when the router operation was upset (reset) due to pulse injection, the router would stop replying to HTTP requests for the configuration setup page (a typical "recoverable loss of function" criterion as might be used in standard system level ESD testing).

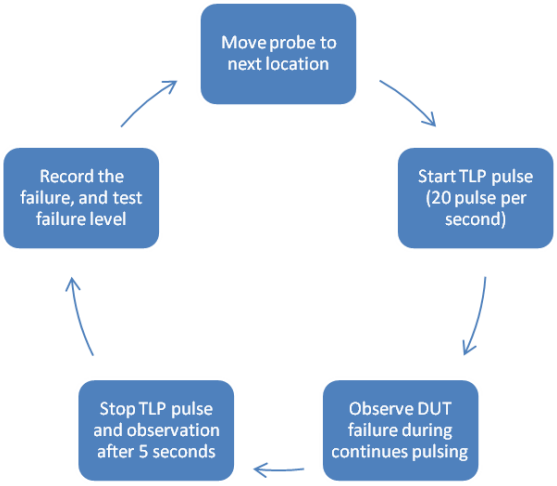


Figure 4: Susceptibility Scanning Step Flowchart

Failure criteria are determined on a system-by-system basis, as they would be with a manual system level ESD testing. In this particular example, the test system repeatedly sends Ethernet requests to the Device Under Test's (DUT's) configuration stack. When the upset occurred in this case, the DUT would hang and stop responding to requests. At this point, the DUT would be reset by the system test controller and move on to the next test point on the grid.

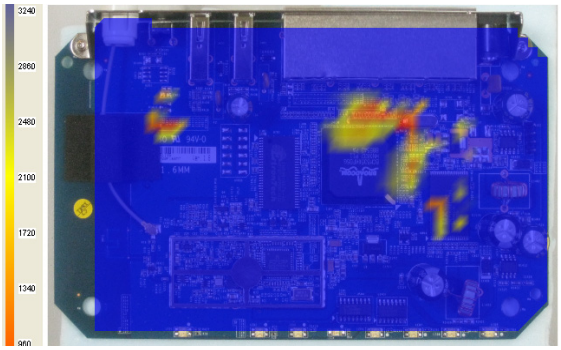


Figure 5: Enhanced color plot of ESD susceptible areas

B. "Current Reconstruction" Testing

In a corollary to the Susceptibility Scanning, the same TLP waveform is injected into a particular I/O port of interest, and the scanning probe is used to "listen" to the PCB.

At each point on the defined grid, the sensed H-field is recorded and processed at a low, non-destructive level creating a new surface plot of energy flow due to the injected pulse. The sensing methodology must take care to sufficiently shield the probe from E-field pickup, and/or remove this component from the measurement capture. [1,7] This does not actually require the system to be functioning, and it may be performed with and without power depending on the failure mechanism to be analyzed. However, the pulse needs to be large enough to trigger the non-linear ESD protection devices, but not so energetic that it causes permanent damage, or a "hard failure" of the system.

This creates a great deal of data which can be post-processed for myriad perspectives on the design.

By trapping the entire pulse at each position, a time variant surface plot can be reconstructed by windowing an interval of interest at various times during the TLP (or IEC or HMM) pulse applied. By post-processing multiple frames with incremental windowing of the pulse, an animated "movie" of the ESD current spreading can be assembled.

In Figure 6, the obvious entry vector of the residual current from the USB port to the SOC ASIC is seen in the upper left corner at the connector where a TVS clamp shunts much of the pulse.

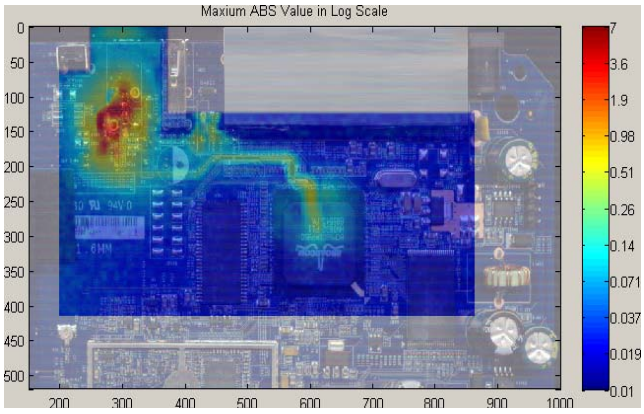
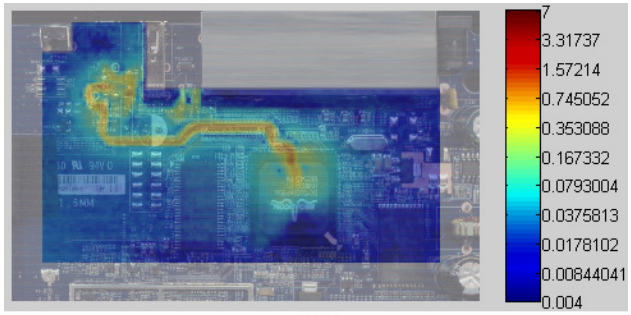


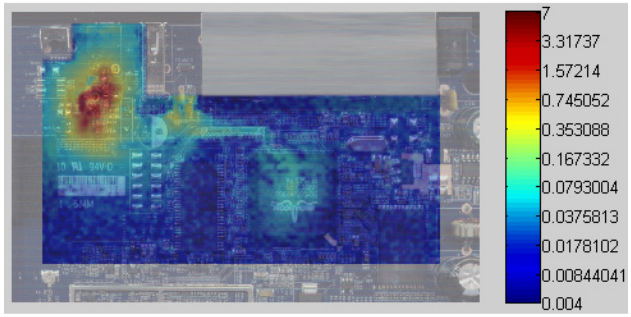
Figure 6: USB Current Spread Scan

Additional analysis can contrast the current reconstruction path with and without a discrete TVS clamp installed. Without the clamp installed (Figure

7a), the current flowing in the signal traces is much higher than with the clamp (Figure 7b), and can be seen coupling into other unrelated, nearby nodes (blue circles.) This may indicate a link into other subsystems if these coupled nodes are related to other susceptible areas identified in the susceptibility scanning.



(a)



(b)

Figure 7: Higher currents carried to integrated on-chip protection (a) than with discrete TVS (b)

This potential problem can then be evaluated or eliminated from consideration by overlaying these plots, and comparing the resulting plots of different selections of TVS devices, layouts or ASIC revisions to determine the ESD robustness of each solution.

For example, the original Susceptibility Scan from Figure 5 is shown here expanded in Figure 8.

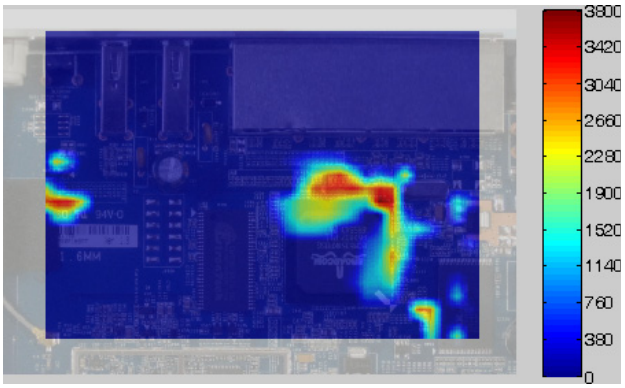


Figure 8: Zoomed ASIC Susceptibility Scan

This plot is then overlaid with the Current Reconstruction Scanning plot of a particular USB port (Figure 9).

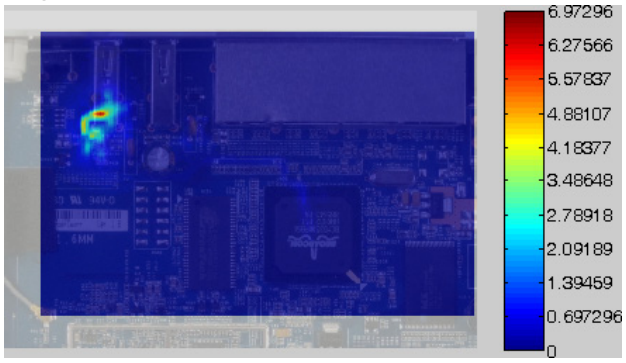


Figure 9: Zoomed Current Spreading Scan via USB port injection

This results in a graphical representation of ESD susceptible areas which can be "reached" externally from that particular USB port (Figure 10).

Figure 10: Overlay of Susceptibility Scan and Injected Current Spread Scan shows USB Port related susceptibility areas and sensitivity levels (*Without TVS – Figure 7a***)**

Repeating this procedure for each I/O port (or other potential system level ESD injection point) yields a new plot (and associated peak susceptibility values and positions on the PCB) for each port or injection point of the system. This does not replace IEC61000-4-2 testing, for example, but rather aides in the debugging of the design when an unexpected susceptibility is discovered.

In Figure 10, the method correctly identifies that the USB pins of the ASIC are of course susceptible to strikes on the USB port. Here, traditional TVS clamping methods can be expected to improve overall

system robustness. However, if the scan overlay indicated that a sensitive DRAM or CLOCK pin was within the area of current spreading from the USB injection port, then the robustness improvement solution might simply require a reoriented layout of the USB and CLOCK/DRAM traces.

Such areas can also unexpectedly be aggravated by migrating the system level ESD protection into the ASIC by driving a larger residual ESD pulse current deeper into the system. The overlaid susceptibility plots for the integrated and external TVS solutions in Figure 7a and 7b can be compared to ensure that the integrated clamping solution does not create other robustness issues elsewhere in the system.

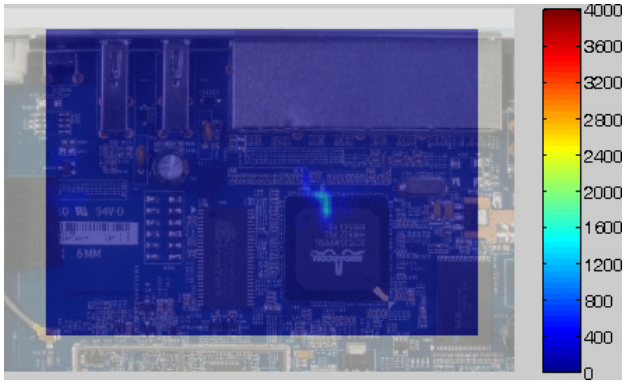


Figure 11: Overlay of Susceptibility Scan and Injected Current Spread Scan shows USB Port related susceptibility areas and sensitivity levels (*With External TVS - Figure 7b***)**

This analysis methodology can be used to help identify, compare and grade the relative improvement of each protection solution to problems at the system level.

Acknowledgements

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