PV Module Diodes TLP Test Report

(Test Service Report Sample)

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ESDEMC
EXPERT ESD/EMC SOLUTIONS

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1 Objective

Bypass and blocking diodes inserted across the strings of the solar panel arrays are found to be susceptible to potential electrostatic discharge (ESD) event. The objective is to explain the theory behind the ESD damage and the proper test and analysis methods for ESD failure of PV module diodes. To demonstrate the proposed test methodology, some diode models supplied by solar panel arrays manufacture were evaluated.

2 Introduction

2.1 Bypass and blocking diodes in Solar Panel Arrays

To help maintain the efficiency and performance of solar panel arrays it is common for bypass diodes to be inserted across individual PV panels, and blocking diodes to be inserted in series with a string of panels that are used in a parallel array (See Fig. 1). Figure 1 demonstrates how these diodes are inserted into a panel array, and the fail scenarios that could happen.

Bypass diodes provide a current path around a shaded or damaged panel, and if these are not installed, the panel will act like a high impedance load when shaded. This effectively reduces the series string output as the current produced by the remaining series connected panels will be forced to go through the shaded panel, thereby reducing the voltage output of the string. If the bypass diodes are installed, and one of them fails due to ESD, it typically fails to a short circuit. When this happens, a scenario, as shown in fig. 1 scenario 1, can occur. The shorted diode does not allow any power produced by its panel to enter the system, thereby lowering system efficiency.

Blocking diodes keep current from the battery pack, or a parallel panel string from entering a damaged string. This is important at night when the panel array cannot provide any power, thus providing a path for the battery to discharge. When installed, the blocking diodes may have leakage current on the order of nano- or micro-amps. However, if they fail due to ESD, they typically fail to a short circuit providing another path for the battery to discharge. This discharge current can be milli-amps or amps. An example of this failure scenario is shown in fig. 1 scenario 2.

Failure of even one of these diodes in the field is very expensive for companies to replace due to the need for a qualified service technician, as most installations will require code requirements to be met. Continued operation of the panel array with a damaged bypass or blocking diode will, at best, hamper the array's efficiency and, at worst, cause permanent damage as it consumes power rather than produces power. It has been proposed that the damage to the diodes is caused by electrostatic discharge (ESD) stress.

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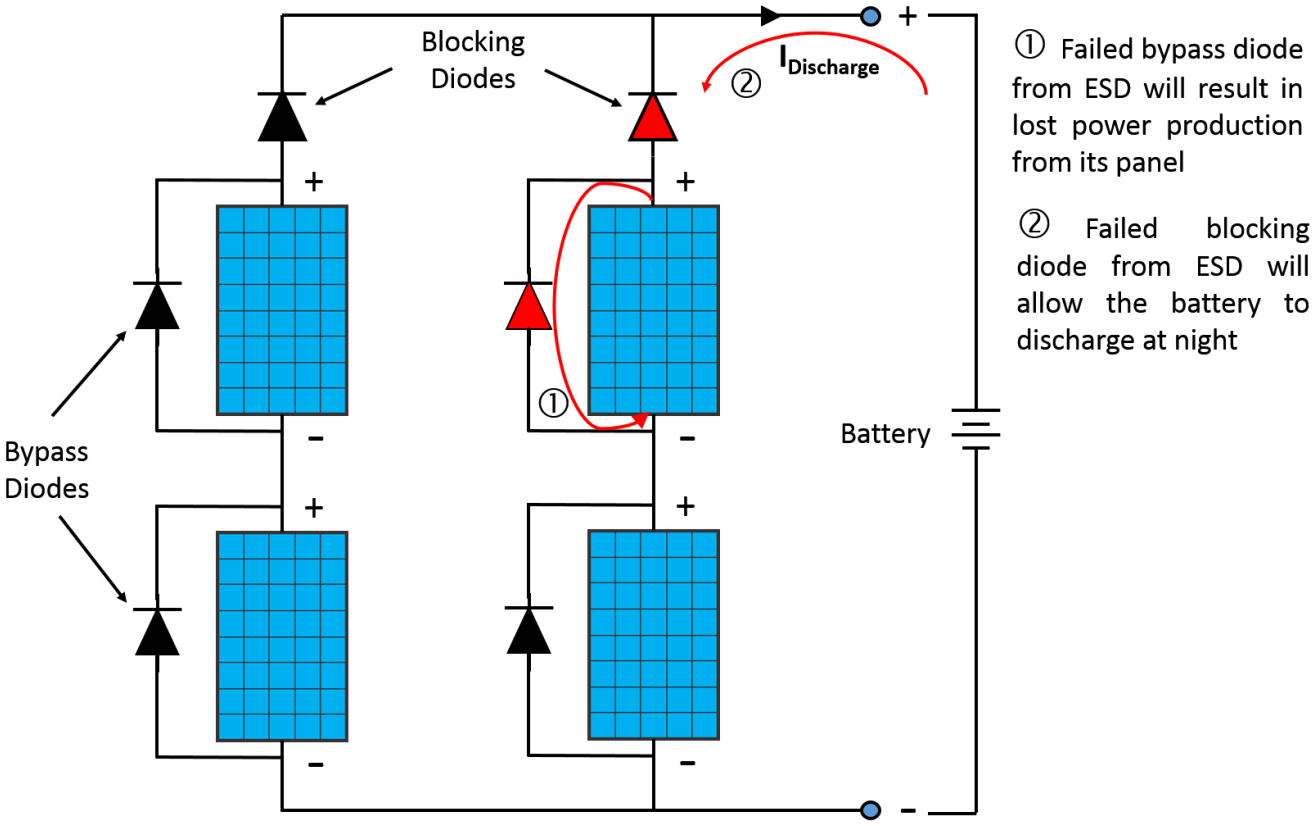

Fig. 1. Solar PV module bypass and blocking diodes connections and fail situations

2.2 How ESD events occur and damage the solar PV module diodes

Human-metal model (HMM), human-body model (HBM) and charged-device model (CDE) ESD most likely occur during PV module diodes junction box assembly. Regarding to solar PV module, the cable connections between the panels can be very long. When the cable is connected to solar panel connection and the cable has existing tribo-electric charge, the potential differential between the cable and solar panel can cause cable discharge event (CDE), resulting the ESD current waveform very different from all cases mentioned above. Because cable connection is an avoidable on-site installation process, cable discharge event should be treated as a special ESD case with special test setup for the PV module diodes quality assurance.

These ESD events describe how an ESD stress event may originate. Underlying physics of these models point to two basic damage causes. Damage may occur as the device cannot withstand the extremely fast voltage transient, or a device is not able to handle the current or the heating caused by the current. Here

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the heating occurs within nanoseconds, such that there is no thermal exchange with the surrounding. Further, the current distribution within the conduction area of the device may not be homogeneous, such that local melting ("filament creation") leads to damage at current levels that the device could handle, if the current would flow with equal current density in the device. Figure 2 demonstrates burn track damage on a Schottky chip caused by ESD. Schottky technology is commonly found in solar PV module bypass and blocking diode manufacturing.

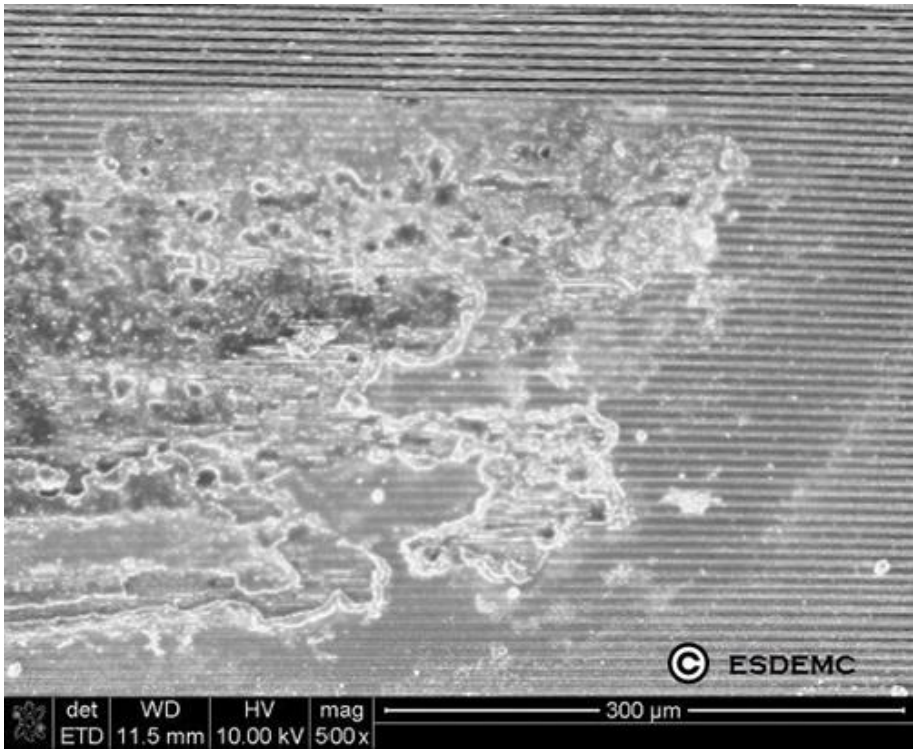

Fig. 2. SEM image of die surface from ESD damaged PV bypass diode sample, melted metal and silicon observed

3 The transmission Line Pulse Test Methodology

Given the nature of how the bypass and blocking diodes could be exposed to and damaged by ESD events, the worst case that would be the Cable Discharge Event, in which both fast rise-time and high energy pulses occur during the installation process. Therefore, based on the existing industrial ESD testing methods, we propose to use the transmission line pulse test method that does not necessarily replace the IEC 61000-4-2 standard, which may have been be used in the current qualification process. Instead, the TLP test method subject a diode (a low resistance DUT) to a faster rise-time and higher energy pulse up to 180A (pulse reflections being allowed to approach the real-world CDE case). This

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provides a fully automated device ESD performance characterization system for transient IV signal and degrade/failure inspection before and after each pulse. Compared to the other types of ESD models, the advantages of using a TLP test are:

(1) Well Defined Consistent Waveform Shape

Both circuit and waveform defined in ESD simulator standards are too flexible (no impedance control for test path, 30% tolerance at only certain time …) This causes ESD simulators to provide very different ESD test results between different test sites. A TLP pulse is very clean and consistent.

(2) Highly Repeatable Test Setup

Fatigue from holding ESD simulator by hand can lead to inconsistent test setups. In TLP testing with Jigs for mounting the DUT, a more controlled test is obtained.

(3) Fast Automatic Measurement and Reporting

Typical TLP testing is done with full automatic control of Oscilloscope Scale Adjustment, Voltage Pulsing, Failure Criteria Checking, and IV Curve update.

(4) Important Device Behavior is recorded for ESD analysis and design

Many useful parameters can be extracted from TLP tests for device transient behavior analysis, modeling and System-Efficient ESD Design (SEED). Traditional ESD tests only generate pulse for Pass/Fail results.

3.1 Test Setup

The TLP test setup is shown in figure 3. A Transmission Line Pulse (TLP) generator provides a rectangular voltage pulse by charging a 50Ω transmission line to a test voltage, and discharging the pulse to the DUT by a special relay which can withstand the voltage, and can switch to an on-‘on ‘status without bouncing. The pulse then travels out of the TLP through a coaxial transmission line where it first reaches a high voltage relay (A621-HVLKR). This relay is capable of withstanding up to 10kV, and is required for the high current TLP testing used with these high power diodes. The relay provides a means of transferring connection of the DUT between TLP Measurement System and the Failure Detection System. In particular, during TLP pulsing, the relay connects the DUT to the TLP, the measurement probes, and the oscilloscope. After each TLP pulse test waveform has been captured, the system switches the DUT to the SMU to measure the diode reverse leakage current at Maximum Recurrent Peak Reverse Voltage (VRRM). The A621-LTKSEM leakage test module also helps to facilitate these connection changes on the low voltage side of the measurement probes.

The DUT current is measured indirectly using a resistive tee to voltage measurement. The current is recovered by the overlapping reflection method. This method measures both the current through and the voltage across the DUT, but for low-resistance devices, such as a diode in the ‘on-state’, this method is not well suited for measuring the device voltage. Instead, the DUT voltage is measured directly at the device, providing a highly accurate voltage probing measurement.

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The current measurement is performed by first measuring the pulse as it passes by the first pick off resistor that goes to Ch1 of the oscilloscope. A short delay later (as determined by the length of coaxial cable between the pick off resistors) the pulse reflected from the DUT is measured at the same pick off resistor yielding an overlapped waveform. Using transmission line theory and a pre-measurement calibration pulse, the current into the DUT can be determined as:

$$IDUT = (V^{+} - V^{-})/Z_0$$

Where V^{+}, V^{-}, and Z_0 are the incident pulse, reflected pulse, and characteristic impedance (50Ω) of the transmission line system, respectively.

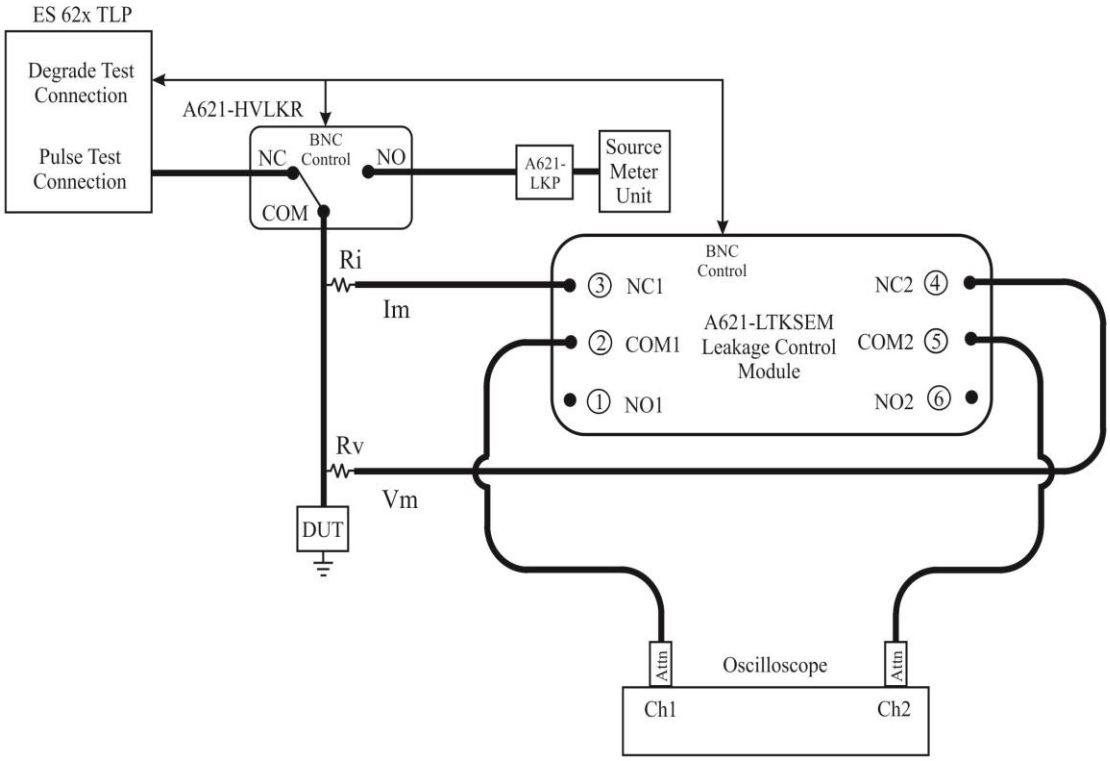

Fig. 3. ESDEMC High current TLP test setup for solar PV module diodes

3.2 Test Procedure

The test procedure is demonstrated in the flowchart shown in Figure 4. Upon entering the test loop, the system measures the leakage current of the DUT to obtain the initial degrade measurement. Next the TLP charge voltage is set. For the testing reported in this article, the charge voltage was set to sweep from 500V to 9600V, in 100V increments. For the first test point, the oscilloscope scale and trigger level are set based on the initial charge voltage and a 50Ω DUT. As testing progresses, the scale and trigger

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level are set based on if the waveforms clip, or is under scaled. If the waveforms do not clip or are not under scaled the settings are kept.

After setting the oscilloscope parameters, the DUT is pulsed and the captured data is compared to the oscilloscope display range for each captured channel to check for clipping and whether the scale is appropriate. If any of the waveforms are clipped, the scale is adjusted and the DUT is pulsed again. If the waveforms are ok, or under scaled, the data is accepted and processed. Any under scaled waveform corrections are made on the next pulse level. Processing is completed by scaling the data by the measurement attenuator and probe values.

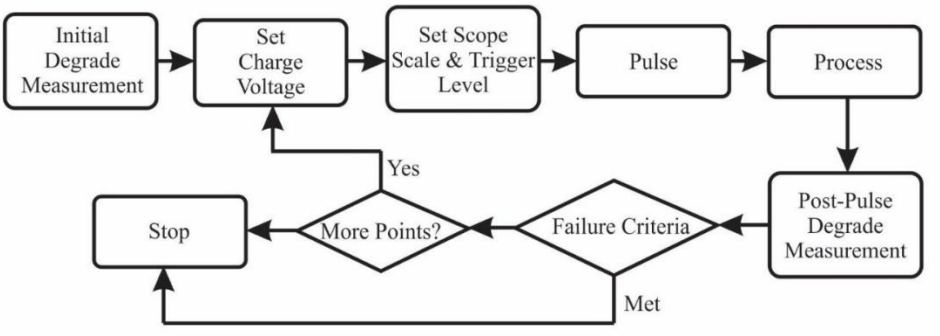

Fig. 4. ESDEMC TLP test procedure flow chart

3.3 Dynamic IV Curve Measurement Principles

One of the goals of the measurement system described above is to obtain the dynamic IV curve of the DUT over the voltage range pulsed. Current and voltage waveforms resulting during pulse test are demonstrated in figure 5. The dashed lines near the end of the pulses represent the start and stop points of the dynamic IV measurement window. The measurement window is typically 70% to 90% range of the pulse, other ranges can also be selected. Over this window, the average value of the time waveform is taken as the current and voltage, respectively. This value is then plotted for each voltage pulse applied.

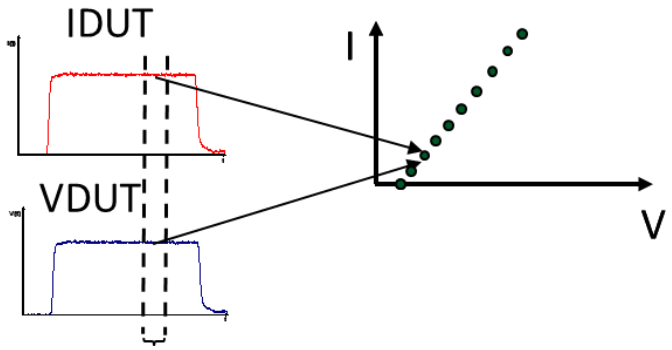

Fig. 5. TLP test dynamic IV curve obtain method

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3.4 Leakage Current Measurement (Degrade/Failure assessment)

The leakage current is measured using the Source Meter Unit (SMU) and, depending on the diode tested, the bias voltage was varied between two and three different voltages with the maximum bias voltage set to the Maximum Recurrent Peak Reverse Voltage (VRRM) for each diode. The VRRM voltage is listed in each individual diodes datasheet.

Also, for the results reported below, for any diode that failed the leakage current limit was set to 2.5mA. This is the compliance limit of the SMU and is not an indicator of diode characteristic after failure, other than they appear to fail to a short.

4 Solar PV Module Diodes Test Cases

ESDEMC Technology has tested several diode models for solar PV module. Here, three diodes models IV curves and leakage currents are shown. The three models have quite different behaviors under TLP test.

4.1 Test settings

PV Module diode TLP test configuration photo and setting see below (Fig. 6 and Table 1). The ES621-200 TLP system was designed for up to 200A high current injection.

The Maximum Peak Repetitive Reverse Voltage (VRRM) of the diodes are: 150V (Diode model #1), 200V (Diode model #2), and 50V (Diode model #3). The VRRM values are important because they provide the maximum bias voltage applied to the diode for leakage current measurement. This value is supplied by the device manufacturer, and can be found in their respective datasheets.

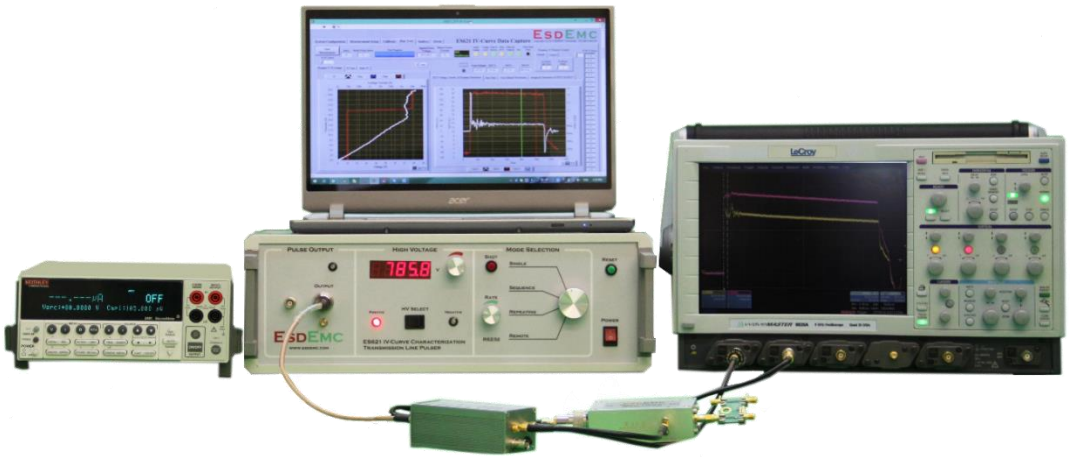

Fig. 6. PV Module TLP Test Configuration Photo

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Table 1 TLP test system settings

Equipment	Brand and Model	Specification and Comments
ESD Test	ES621-200 TLP System (A specially developed TLP system, not a release model. The ES620-200PVD model may be released for a simplified turnkey solution)	<=1 ns rise-time, 100 ns pulse width, Max 10 kV charge line with no reflection rejection. The 10 kV charge voltage is achievable in the real world under dry conditions. The 100 ns pulse is represented approximately 10 meters of cable that is very close to the grounding conduit. Please note that during installation, a charged PV module connecting to a grounded cable will have the same effect as a charged cable discharging to a PV module. A 10 meter cable may not be the worst case since solar cables could be up to hundreds meters for certain systems.
Failure Test	Keithley Model 2400 or Keithley Model 6487	This configuration depends on the diode VRRM
Oscilloscope	Agilent DSO9204H	2 GHz, 10 Gs/s (200 MHz min bandwidth per ANSI/ESD STM5.5.1-2014 standard)

4.2 Diode model #1, 150V VRRM

Out of the 80 pieces diode model #1devices tested, no failure occurred. The Dynamic IV and Leakage Current curves for three samples are shown in Figure 7. The Dynamic IV curve is read from the Y-axis to the bottom of the X-axis, and the Leakage Current from the Y-axis to the top of the X-axis, see the circle marks in the figure. Note that the top of the X-axis is logarithmic due to the dramatic change in leakage current once a device fails to a short circuit.

In the figure, three leakage current curves have no change, means there was no failure during TLP test up to about 200A current injection. But the dynamic IV curves could not overlap, which means that the repeatability of Diode model #1 is not good enough.

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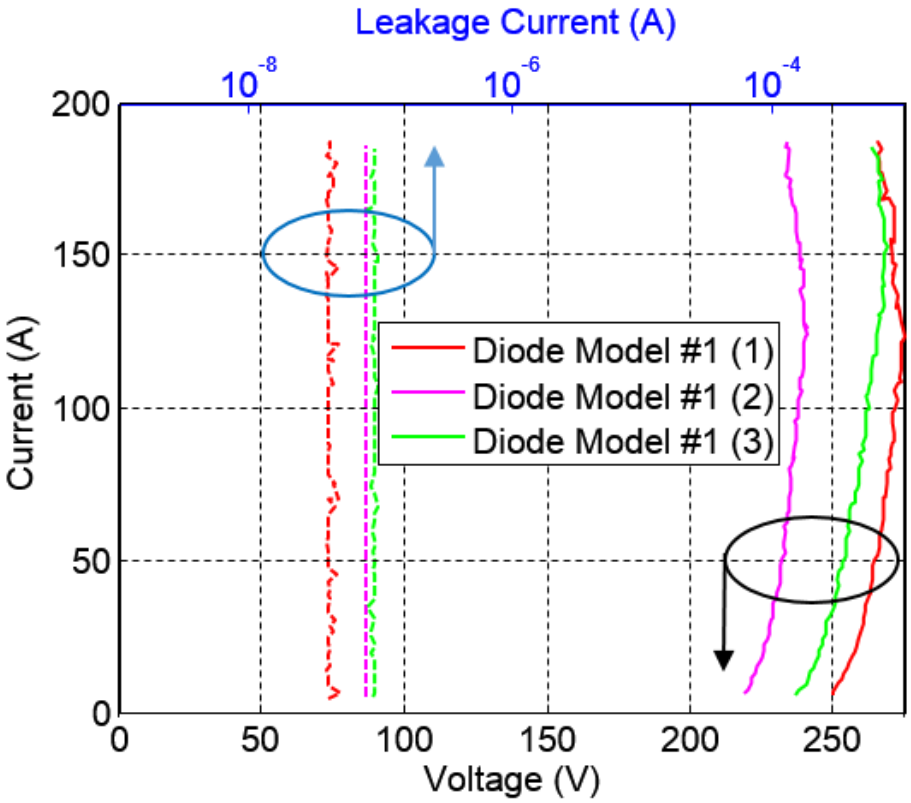

Fig. 7. Diode model #1 dynamic IV and leakage current curves.

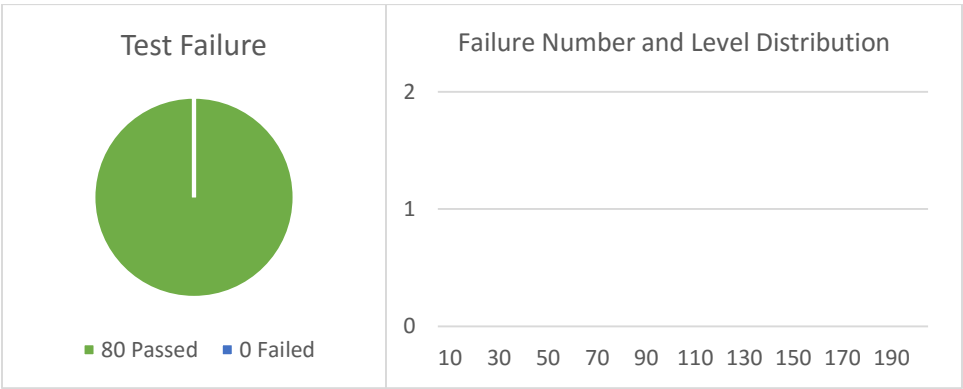

Fig. 8. Diode model #1 Failure Rate @ High Current TLP Test

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4.3 Diode model #2, 200V VRRM

The Diode model #2 had eleven failures out of eighty diodes tested. The Dynamic IV and Leakage Current curves, for three of the failed diodes, are shown in figure 9, and the minimum, maximum, and average pulse current for each of them are listed in figure 10.

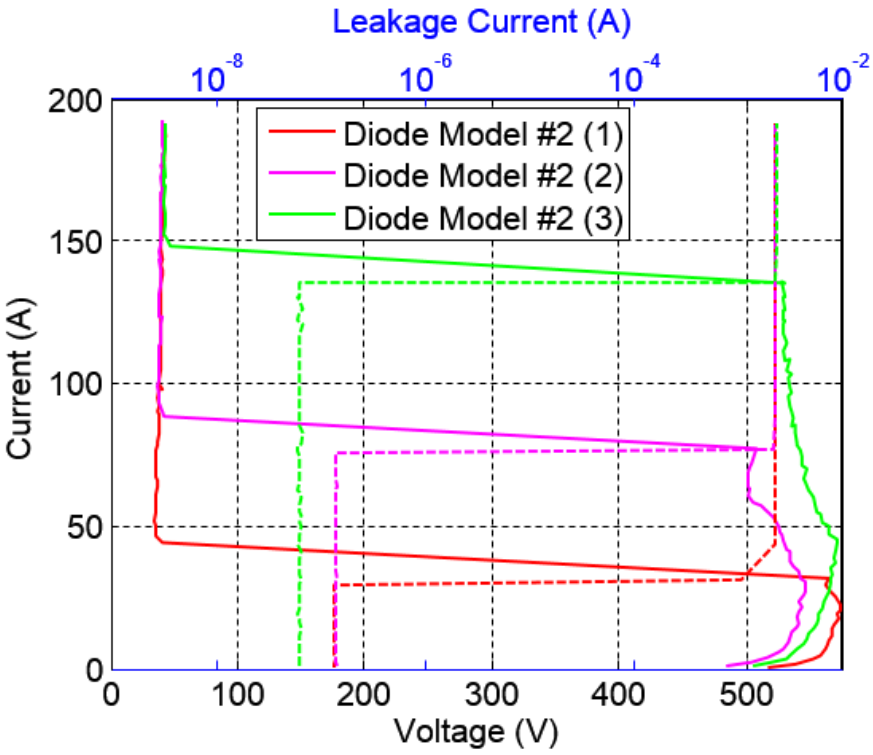

Fig. 9. Diode model #2 dynamic IV and leakage current curves.

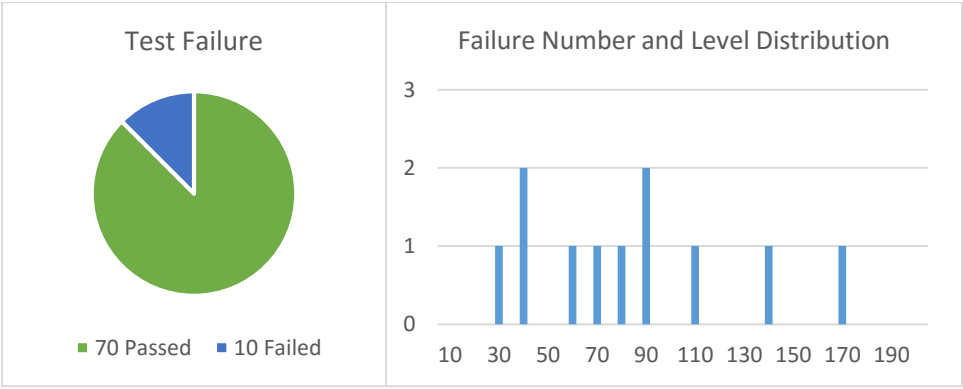

Fig. 10. Diode model #2 Failure Rate @ High Current TLP Test

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4.4 Diode model #3, 50V VRRM

All of the diode model #3 failed in the TLP test. The Dynamic IV and Leakage Current curves, for three of the failed diodes, are shown in figure 11, and the minimum, maximum, and average pulse current for each of them are listed in figure 12.

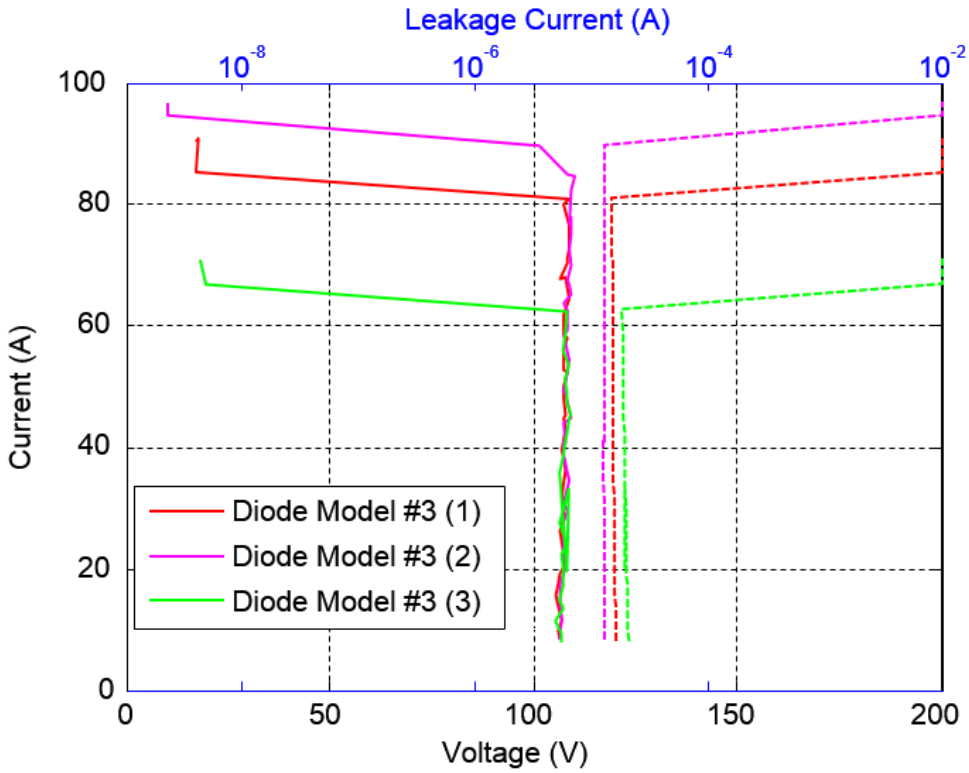

Fig. 11. Diode model #3 dynamic IV and leakage current curves.

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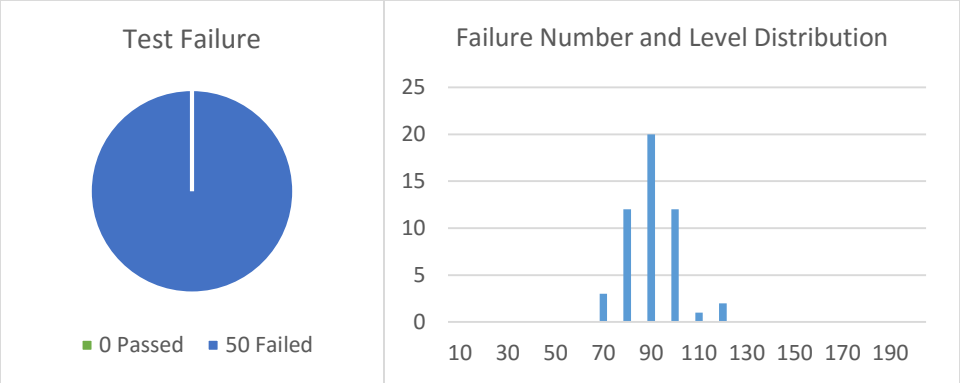

Fig. 12. Diode model #3 Failure Rate @ High Current TLP Test

5 Conclusion

According to our customer, diode failure rate through TLP test methodology correlates to their field return failure rate. Therefore, we recommend that TLP testing be performed for the purpose of solar PV module diodes evaluation or quality control In addition, it may be in the best interest of both solar PV module and diode manufacturers to investigate the quality control of the diodes selected, yielding a more reliable design for field use.

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