Introduction of Transmission Line Pulse (TLP) Testing for ESD Analysis - Device Level
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What is ESD?

- Electrostatic Discharge (ESD) is an exchange of charge between two objects. It occurs when contact is established or if the dielectric breakdown of the material between the two objects is exceeded.

Table 1: Static Voltage Generation Examples (Source: ESD Association)

<table>
<thead>
<tr>
<th>Examples of Static Voltage Generation At Different Levels of Relative Humidity (RH)</th>
<th>10-25% RH</th>
<th>65-90% RH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Means of Generation</td>
<td>35,000 V</td>
<td>1,500 V</td>
</tr>
<tr>
<td>Walking across carpet</td>
<td>12,000 V</td>
<td>250 V</td>
</tr>
<tr>
<td>Walking across vinyl tile</td>
<td>6,000 V</td>
<td>100 V</td>
</tr>
<tr>
<td>Worker at bench</td>
<td>20,000 V</td>
<td>1,200 V</td>
</tr>
<tr>
<td>Chair with urethane foam</td>
<td>18,000 V</td>
<td>1,500 V</td>
</tr>
</tbody>
</table>

Note: The voltages are relatively high, some of them may occur under some extreme cases.
Why do we care about ESD?

- Potential damage to circuit designs, leading to:
  - Poor product quality
  - Angry customers
  - Increased costs for repair and rework
- Components permanent damage by breakdown, or oxide punch through, excessive local heating as components may not be able to dissipate the energy fast enough

Source: 2005 ESD/EOS Symposium paper
Hard failure - IC Damages from ESD

RS-232 interface IC after an ESD strike of 15kV
Physical Damage, Still Functional - IC Damages from ESD

ESD overvoltage surge. Still operable but close to total failure.
Hard failure - IC Damages from ESD

EOS (Electrostatic Over Stress) Damage

Figure 2-3: Shown on the left is a SEM image of good transistor. To the right is a SEM image showing EOS damage (indicated by yellow arrows).
How can we protect against ESD?

1. Controlled Environment
   - Reduce the potential for charge build up
   - Grounded equipment and furniture
   - Clean Room - Controlled humidity and particles
   - Does not help when system is shipped to End-User, such as Consumer Electronics.
2. Improve System ESD Robustness

• Understand system working environment and potential ESD risks
• Design your system with careful ESD protection strategy!
  • Understand ESD sensitivities of critical components
  • Test and choose best ESD protection solutions for weakness
  • Test and further improve system level ESD robustness

Design engineers need critical data from different types of ESD tests. TLP test is a very powerful tool that provides many important data for ESD design!

Graph 1

Graph 2
How do we test for ESD robustness?

- **Human Body Model (HBM)**
  - Charged human body contact with device under test (DUT)
  - ANSI/ANSI/ESDA/JEDEC JS-001-2010
  - Test to 4000V, < 3A into a short (8000V optional)
  - Discharge from the skin (IEC 61000-4-2 is a discharge from a metal part)

Rise Time ($t_r$) for short – 2 to 10ns

Decay Time ($t_d$) for short – 130 to 170ns
How do we test for ESD robustness? Cont’d

- Machine Model (MM) \(^3\) (MM model is used very little)
  - Charged machine discharge to devices, such as during production
  - ESD STM5.2-2012
  - Test to 400V
  - < 7A into a short

Major Pulse Period \(t_{pm}\) for short – 66 to 90ns
How do we test for ESD robustness? Cont’d

• Charged Device Model (CDM)\(^4\)
  • Charged device discharge to other metal parts or ground plane, such as an integrated circuit during assembly
  • ESD S5.3.1-2009
  • Device is charged via a charging plate
  • Non-contact discharge as grounded object approaches a charged pin
  • Test to 2000V
  • 30A (4pF verification module, 260ps rise time)

Rise Time \((t_r)\) – \(~200\)ps, Full Width Half Height \((t_{dh})\) - \(~400\)ps
How do we test for ESD robustness? Cont’d

- IEC 61000-4-2:2008
  - Charged human body contacting a DUT with a metal, discharging to a system
  - System level test

<table>
<thead>
<tr>
<th>Level</th>
<th>Indicated voltage</th>
<th>First peak current of discharge (±15 %)</th>
<th>Rise time ( t_r ) (±25 %)</th>
<th>Current (±30 %) at 30 ns</th>
<th>Current (±30 %) at 60 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>7.5</td>
<td>0.8</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>15</td>
<td>0.8</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>6</td>
<td>22.5</td>
<td>0.8</td>
<td>12</td>
<td>6</td>
</tr>
<tr>
<td>4</td>
<td>8</td>
<td>30</td>
<td>0.8</td>
<td>16</td>
<td>8</td>
</tr>
</tbody>
</table>

The reference point for measuring the time for the current at 30 ns and 60 ns is the instant when the current first reaches 10 % of the 1st peak of the discharge current.

NOTE The rise time, \( t_r \), is the time interval between 10 % and 90 % value of 1st peak current.

Contact discharge current waveform parameters

Ideal contact discharge waveform (4kV)

IEC Test Configuration
How do we test for ESD robustness? Cont’d

- Human Metal Model (HMM) \(^6\)
  - Charged human discharging through a metal tool
  - ANSI/ESD SP5.6-2009
  - **Component** level test similar to IEC 61000-4-2
  - Current waveform parameters same as IEC 61000-4-2
  - Can use **TLP** and the 50Ω arrangement for more reliable and automatic failure detection testing

![Setup A](image1)

![Setup B](image2)

50Ω Coaxial Source Setup

![Diagram](image3)
What is TLP Measurement?

- **Transmission-Line Pulse (TLP) Measurement** is a methodology to test and study integrated circuit technologies and circuit behavior in the time domain of transient events, such as Electrostatic-Discharge (ESD), Cable Discharge Event (CDE).

- **History:**
  - Due to interest in Electromagnetic Pulse environments, Wunsch and Bell studied **pulsed power failures in semiconductor junctions** in the 1960’s.  
  - Also developed in the 1960’s, by Bradley, Higgins et.al., was the use of charged transmission lines to generate rectangular pulses. 
  - In the 1980’s the idea of using Transmission Line Pulsing for modeling of ESD phenomena was introduced by Maloney and Khurana. 
  - The first commercial TLP system was introduced by Barth Electronics in the mid-1990’s.
What is TLP Testing?

TLP Standard Requirements

- **Standard TLP (STM5.5.1-2014)**
  - Typically 0.2 to 10 ns rise time
  - 10ns to > μs pulse width (100ns typical)
  - Minimum of 200MHz BW oscilloscope
  - Minimum of 200MHz BW voltage probe
  - Minimum of 200MHz BW current probe

- **Very Fast TLP (SP5.5.2-2007)**
  - Typically <= 200 ps rise time
  - 1 to 10ns pulse width
  - Minimum of 2.5GHz BW oscilloscope with 5GSa/s sampling
  - Minimum of 1GHz BW voltage probe
  - Minimum of 2GHz BW current probe
What is TLP Testing? Cont’d

- A basic pulse generator consists of a charge line (TL1) of length L, a switch (S1), and a High Voltage power supply (Vo).

- The length of the charge line determines the pulse width.
- Standard TLP typically uses 100ns pulse width, and a 1ns rise time.
- Pulses are incrementally increased until failure, or the maximum voltage is reached.
- Failure typically determined by DC leakage current measurement.
- Measurement window is typically between the 70 to 90% region to obtain a point of the I-V curve.

Graph 5
What is TLP Testing? Cont’d

- I-V Characterization of TVS diode (70% to 90% window) measurement
What is TLP Testing? Cont’d

- I-V Characterization of TVS diode (70% to 90% window) measurement
- 100ns Pulse

Semtech uClamp0541Z Datasheet

ESDEMC TLP Measurement
What is TLP Testing? Cont’d

• VF-TLP Measurement: turn on behavior of a TVS diode (first few nano-seconds of pulse)

RDUT vs. Time vs. Pulse Voltage Waterfall

6 V TLP Pulse

Upper RDUT value limited for plotting purposes
Typical Standard TLP Applications

1. Use TLP to obtain pulsed I-V curve, e.g. **Get Protection Device Dynamic Resistance**
   (Dynamic Resistance is defined as dV/dI of the I-V curve)

   \[
   R_{\text{dyn}} = \frac{(V_t2 - V_t1)}{(I_t2 - I_t1)}
   \]

   Dynamic resistance is a very important specification for ESD protection device. The lower the \( R_{\text{dyn}} \), the more ESD current flows through the protection device and less current flows through protected device.

   - Transient Voltage Suppressor – 100’s of milli Ω’s to Ω’s
   - Multi-Layer Varistor – Ω’s or more for low capacitance devices
Typical Standard TLP Applications

2. Use TLP and auto failure check setup to test device ESD robustness / sensitivity

ESD Robustness of System / IC / Module are often evaluated with different ESD test setups. Some failure types due to transient high energy damage can be simulated with controlled rise-time / pulse-width rectangle TLP pulses or RC circuit discharging into matched 50 Ohm system waveform. TLP test results have been used to estimate HBM, IEC 61000-4-2, HMM failure level. n

Eg, ESD thermal failure correlations*\textsuperscript{(Note)}: TVS IEC 1 kV level = 2 A, 100 ns TLP pulse level

IC HBM 1 kV level = 1.5 A, 100 ns TLP pulse level

Please refer to publications for TLP test correlations usage, different device has different sensitivities!

- Correlation between transmission-line-pulsing I-V curve and human-body-model, Jon Barth, John Richner
- ESD Relations between system level ESD and (vf-)TLP, T. Smedes, J. van Zwol, G. de Raad, T. Brodbeck, H. Wolf
- A TLP-based Human Metal Model ESD-Generator for Device Qualification according to IEC 61000-4-2, Yiqun Cao 1, David Johnsson 1, Bastian Arndt 2 and Matthias Stecher
- Pitfalls when correlating TLP, HBM and MM testing, Guido Notermans, Peter de Jong and Fred Kuper
- A Failure Levels Study of Non-Snapback ESD Devices for Automotive Applications, Yiqun Cao, Ulrich Glaser, Stephan Frei and Matthias Stecher
- Correlation Between TLP, HMM, and System-Level ESD Pulses for Cu Metallization, Y. Xi, S. Malobabic, V. Vashchenko, and J. Liou
- Capacitive Coupled TLP (CC-TLP) and the Correlation with the CDM, Heinrich Wolf, Horst Gieser, Karlheinz Bock, Agha Jahanzeb, Charvaka Duvvury, Yen-Yi Lin

\textit{Note:} 1. Standard TLP doesn’t give first peak kind of pulse as IEC61000-4-2, so device failures during first peak can not repeat TLP tests. VF-TLP can provide fast rise-time and short pulse to approach the event.

2. Standard TLP are based on 50 Ohm impedance, while other ESD model are based on different impedance system so the voltage applied before device fully turn-on could be very different and cause different failure types.
100ns TLP with <=200ps rise time, Overlap TDR measurement method was used

The snapback is due to Rdut has changed during the 100 ns pulse stressing
Electrical Safe Operating Area of N-ch MOSFET

Safe operating area (SOA) is an important electrical property to understand the ESD/EOS transient limitation of a component.
Typical Standard TLP Applications

4. Characterize device turn-on/off transient characteristic (the 3D waterfall plots)  
   e.g. ESD protection device react speed

5. Characterize device Charge recovery effects  
   e.g. reverse and forward recovery of diodes

6. Characterize device linearity under pulsed transient  
   e.g. capacitance changes over high voltage

7. Characterize device break down effects  
   e.g. Touch panel sensor traces sparking / fuse effect during ESD

8. Characterize saturation effects on common mode chokes and Ethernet magnetics

9. Measure the non linearity of capacitance of Multi-Layer capacitors
    ....

• Note, there are more system level applications of TLP will be covered in another PPT release in 2015 Q2,  
  please contact us if you needed it.
What is TLP Testing? Cont’d

- **Very Fast TLP (VF-TLP)**
  - Commonly used for characterizing device Clamping Speed and Gate Oxide Punch Thru
  - Pulse widths are very narrow (< 10ns)
  - Rise times are at least 15% of Pulse Widths (100 ps to 500ps) at least? Or less than?
  - A VF-TLP measurement setup (typically a low loss delay line with wide-bandwidth voltage pick-up T, or a wide-bandwidth directional coupler or a pair of wide-bandwidth direct I and V probes very closely positioned DUT, etc… ) is build so that the incident and reflected pulses can be measured separately and precisely
  - De-embedding of the cable loss is necessary and performed using frequency domain techniques

![A Typical VF-TLP Measurement Setup with Delay Line](image-url)
Ultra Fast VF-TLP Pulse

ESDEMC ES621 VF-TLP Waveform with 60 ps rise-time, 1ns pulse width
Measured with 18GHz Cable/ATT + 23 GHz/100Gs Scope Tek MSO 72304DX
What is TLP Testing? Cont’d

- Use TLP to Check ESD Protection Circuit **Peak Pass Through Voltage and Clamping Voltage**

  - Peak voltage is the initial response to the pulse edge rate
  - Clamping voltage is the output voltage when protection device fully turns on and clamps
  - Some sensitive device are sensitive to short time peak voltage (high E-field strength), therefore both parameters are important to understand the device sensitivity and design best ESD protection solution.
# ESD Robustness Tests vs. TLP Testing (Pulse Shape Parameters)

<table>
<thead>
<tr>
<th></th>
<th>HBM</th>
<th>MM</th>
<th>IEC (2nd Peak)</th>
<th>IEC (1st Peak)</th>
<th>CDM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical max Peack V*</td>
<td>4000V</td>
<td>400V</td>
<td>8kV (contact)</td>
<td>2000V</td>
<td></td>
</tr>
<tr>
<td>Typical max Peack I*</td>
<td>&lt; 3A (short)</td>
<td>&lt; 7A (short)</td>
<td>16A (@30ns)</td>
<td>30A</td>
<td>30A</td>
</tr>
<tr>
<td>Rise Time*</td>
<td>2 – 10ns</td>
<td>~ns – 10ns</td>
<td>~ns</td>
<td>800ps</td>
<td>&lt; 200ps</td>
</tr>
<tr>
<td>Pulse Width*</td>
<td>130 – 170ns</td>
<td>66 – 90ns</td>
<td>~100ns</td>
<td>~5ns</td>
<td>&lt; 400ps</td>
</tr>
<tr>
<td>Pulse shape compatible with</td>
<td>Standard TLP</td>
<td>Standard TLP</td>
<td>Standard TLP</td>
<td>VF-TLP</td>
<td>VF-TLP</td>
</tr>
<tr>
<td>Typical Failure Modes</td>
<td>Junction damage, metal penetration, melting of metal layers, contact spiking, gate-oxide damage</td>
<td>Junction damage, melting, gate-oxide damage</td>
<td>Melting failure</td>
<td>Oxide punch through</td>
<td>Gate-oxide damage, charge trapping, junction damage</td>
</tr>
</tbody>
</table>

* Typical values noted in each respective standard.
Benefits of TLP testing vs. other ESD tests

• Well Defined Consistent Waveform Shape
  • Both circuit and waveform defined in ESD simulator standards are too flexible (no impedance control for test path, 30% tolerance at only certain time ...) This cause ESD simulators to provide very different ESD test results between different test sites. TLP pulse is very clean and consistent.

• Highly Repeatable Test Setup
  • Fatigue from holding ESD simulator with hand leads to inconsistency setup, vs TLP test with Jigs for mounting components give a more controlled test.

• Fast Automatic Test, Measurement and Report !
  • Usually TLP test is done with full automation control of Pulsing, DC Leakage, I-V Curve real-time update and automatic failure detection

• Important Device Behavior is recorded for ESD analysis and design !
  • Many useful parameters can be extracted from TLP tests for device transient behavior analysis, modeling and System-Efficient ESD Design (SEED). However traditional ESD tests only generate pulse for P/F results.
General Testing Procedure

• SOZL (Short – Open – Zener – Load) Calibration (only if change setup)
  • Short and Open measurements provide Series and Shunt resistances, respectively
  • Zener and Load measurements provide Voltage and Current correction factors, respectively
  • This calibration should be performed every few months or if equipment is changed
• Test standard for comparison
  • Measure a well known device for comparison
• Reporting
  • Pulse width
  • Rise time
  • Failure type, and level (DC Leakage, Fusing, Snapback)
  • Pulse Level, DUT Voltage, and DUT Current at failure
  • Dynamic Resistance if applicable
  • Snapback (eSOA)
TLP System Configuration Considerations

- **What applications you want to test with TLP?**
  - Evaluate ESD protection devices performance (Compare $R_{dyn}$ and Clamping speed)
  - Evaluate ESD failure level of device and module
    - Different pulse shape (TLP, HMM, HBM etc...) or pulse-width, rise-time might needed, and wide range of current injection level (40A, 90A, 160A etc...)
  - Evaluate Safe Operation Area
    - A wide range of different pulse-width selection and injection level is needed.
  - Touch panels breakdown and fuse sensitivity
    - Differential Pulse injection and measurement

- **What equipment will you need to configure?**
  - Pulse generator – TLP / VF-TLP / HMM / HBM etc...
  - Device probing method? – PCB with SMA connector, IC test jig, probe station
  - Single-end or differential Injection? --- HV wideband splitter & Inverter
  - Current and Voltage measurement method – direct probes
  - Transient data capture – Oscilloscope (bandwidth depends on application)
  - Bias and DC measurement -- SMU / Power Source / Picoammeter
TLP Systems Specification on Market

- Standard TLP System
  - Recommend spec: 2 kV open voltage / 40A short current
  - ESDEMC Standard TLP Solution currently provides up to 7kV / 140A, the highest pulse injection and IV measurement specification in the world)
  - Nearest competitors: 4kV / 80A, Others 2kV / 40A

- VF-TLP System
  - Recommend spec: Injection level up to 1kV / 20A, with clean, fast and stable rise-time (<=100 ps), very wide analogue measurement bandwidth (2.5 ~ 4 GHz) and advanced digital frequency compensation
  - ESDEMC VF-TLP Solution currently provides
    - TLP Pulse up to 1kV / 20A with 60 ps rise-time and up to 5 kV / 100 A with 200 ps rise-time
    - Measurement with up to 6 GHz analogue bandwidth measurement capability plus all port frequency compensation algorithm using Network Analyzer S-parameters
World’s Top Specification TLP Dynamic IV-Curve Solution

2011 Beginner in IV-TLP Solutions
2013 Matching Top Spec System
2014 One of the best IV-TLP System

<table>
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<th>Specifications/Functions</th>
<th>ESDEMC ES620/ES621</th>
<th>Other Brand Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fastest Rise-time</td>
<td>About 60 ps (World’s fastest)</td>
<td>100 ps, 200 ps</td>
</tr>
<tr>
<td>Longest Pulse-width</td>
<td>2000 us (1ms under development)</td>
<td>1600 us, 400 ns</td>
</tr>
<tr>
<td>Maximum Current Injection Level</td>
<td>160 A</td>
<td>80 A, 40A, 30A...</td>
</tr>
<tr>
<td>Standard 2D IV Curve Analysis</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Advanced 3D IVT Curve Analysis</td>
<td>Yes, currently unique</td>
<td>No, need additional work</td>
</tr>
<tr>
<td>Voltage Measurement Methods</td>
<td>Resistive Direct, Overlap TDR, Non Overlap TDR</td>
<td>Usually only 1 or 2 types</td>
</tr>
<tr>
<td>Current Measurement Methods</td>
<td>Resistive Direct, Resistive Equation, Inductive Direct, Overlap TDR, Non Overlap TDR</td>
<td>Usually only 1 or 2 types</td>
</tr>
<tr>
<td>Error Correction Methods</td>
<td>SOLZ Correction, All ports S-parameters compensation, Trigger timing alignment</td>
<td>SOLZ Correction</td>
</tr>
<tr>
<td>Differential TLP Pulsing and IV Test</td>
<td>Yes, unique</td>
<td>No</td>
</tr>
</tbody>
</table>
General FAQ for TLP testing?

• How much does TLP system cost?
  • Most TLP system in the market current cost about 80 ~ 250 K USD
    • ESDEMC provides ES620 Ultra-portable and low-cost version system cost about 80 – 200K
    • ESDEMC guarantee to provide better capability TLP system at same cost of other competitors

• Can customer use their equipment for TLP system configuration?
  • Most TLP system in the market doesn’t support wide range of instruments, but ESDEMC TLP software designed with great compatibility in mind, you can choose most equivalent instruments you had (Agilent, Tek, Lecroy, Rigol, Keithley, etc…). You change instrument settings in few clicks or contact us if you need support!
General FAQ for TLP testing?

- **What bandwidth is really needed for TLP testing?**
  - This really depends on the IV measurement window you want to measure, for most applications with standard 100 ns TLP, 200+ MHz bandwidth is fine if you only check the 70-90% of 100 ns pulse window for Rdyn and pulse failure level, even ESDA TLP standard require higher bandwidth.
  - However if customer want to measure the device characteristic from the first ns of the pulse injection, VF-TLP generator with very clean and stable edge and 4~8 GHz oscilloscope is recommended.
Thank you!

- Please feel free to contact info@esdemc.com for questions about general ESD test and applications, we are expert in this field and we like to help!

- We will keep updating this ppt and we offer FREE application consulting. We also send out latest technical notes and sales promotion each quarter, please email us if you like to subscribe.

- If you are interested, below are few slides about ESDEMC Technology LLC
To be one of the best Commercial Solution Providers in the field, by ESD/EMC Engineers, for ESD/EMC Engineers
Development Achievements (2011.03 to present)

**ESD/Transient**
- World’s top spec Transmission Line Pulse System (TLP/VFTLP)
- World’s first Commercial Cable Discharge Event (CDE) System
- ESD Simulator, ESD Targets, Adapter Line
- Plus additional features...

**EMC/RF**
- Microwave Material Characterization System (5-22 GHz)
- IC Strip TEM Cell (4kV/ DC-5.5 GHz)
- Wideband RF Amplifiers (Up to 40 GHz)
- Wideband Power Amplifier (4GHz/25W )
- Plus additional features...

**Other Key Products**
- Wideband HV Pulse Attenuator (Symmetric, 4kV / 3.5GHz)
- Oscilloscope ESD Protector (up to 6 GHz)
- HV Pulse Differential Splitter (1MHz to 2GHz)
- See website ESDEMC.COM for more products
Some Previous Customers (2011 to 2013)

- Apple
- Bosch
- Bose
- Cisco
- Samsung
- LG
- SunPower
- HP
- HaeFely EMC Technology
- Tektronix
- Thermo Fisher Scientific
- TDK RF Solutions Inc.
- NXP
- General Dynamics
- NASA
- Lockheed Martin
- Motorola Solutions
Niche: Solutions by ESD/EMC experts, innovative & flexible, focused on ESD/EMC design, analysis and debugging

Growth: 2010.09 Business setup in Founder’s home
         2011.03 to now Group of 5 professionals

ESDEMC is strategically located in the same facility with the world’s largest academia EMC research group MS&T-EMCLAB
We can improvise...

We are growing ...

Oh, I have a new idea ...

I can do it ...

Fredric Stevenson
Business/Technical Development

David Pommerenke
Chief Technology Consultant

Wei Huang
Founder/Owner
Chief Design Engineer

Jerry Tichenor
Design Application Engineer
References


References Cont’d


Graph 5 & 6: Reference 10


