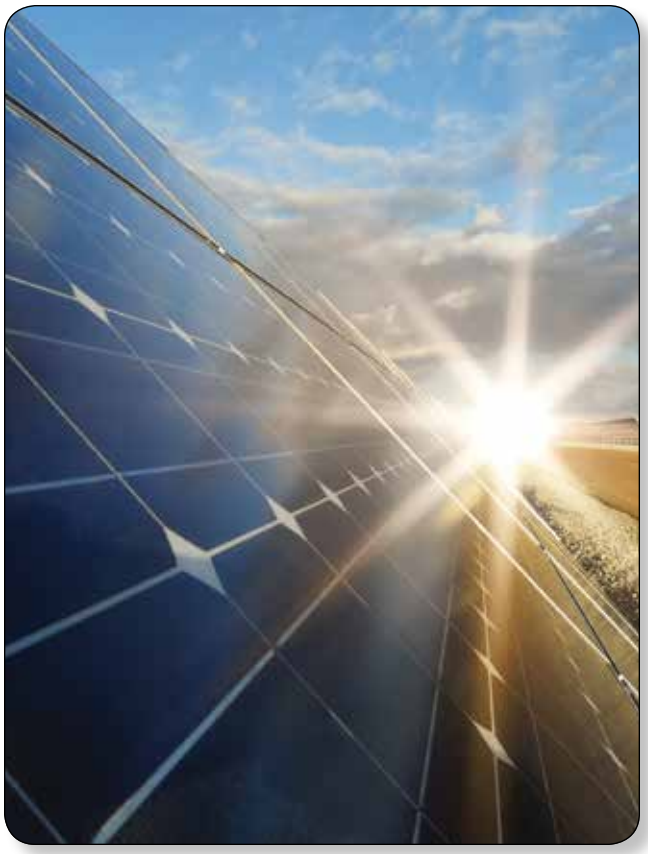
ESD Failure Analysis of PV Module Diodes and TLP Test Methods

BY WEI HUANG, DAVID POMMERENKE AND JERRY TICHENOR



Bypass diodes inserted across the strings of the solar panel arrays are essential to ensure the efficiency of the solar power system. However, those diodes are found to be susceptible to potential electrostatic discharge (ESD) events in the process of solar photovoltaic (PV) panel manufacture, transportation and on-site installation. Please refer to [1], where an International PV Module Quality Assurance Forum has been set up to investigate PV module reliability, and Task Force 4 has been setting guidelines for testing the ESD robustness of diodes used to enhance PV panel performance.

This article explains the theory behind the ESD damage and the proper test and analysis methods for ESD failure of diodes. To demonstrate the proposed testing methodology that follows, we will be evaluating six different types of diode models as supplied by our customer, who manufactures solar panel arrays.

BACKGROUND

Bypass and Blocking Diodes in Solar Panel Arrays

To help maintain the efficiency and performance of solar panel arrays it is common for bypass diodes to be inserted across individual PV panels, and blocking diodes to be inserted in series with a string of panels that are used in a parallel array (see Figure 1). The bypass diodes provide a current path around a shaded or damaged panel. If these are not installed, the panel will act like a high impedance load

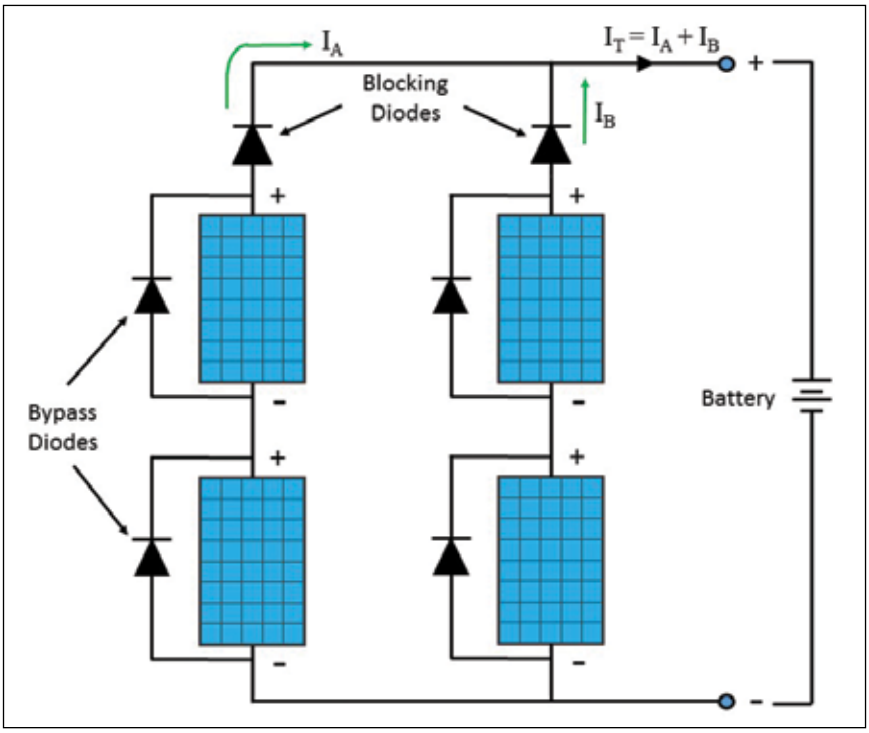


Figure 1: Solar PV module bypass and blocking diode connections

when shaded. This effectively reduces the series string output as the current produced by the remaining series connected panels will be forced to go through the shaded panel, thereby reducing the voltage output of the string.

If the bypass diodes are installed, and one of them fails due to ESD, it typically fails to a short circuit. When this happens (see Figure 2), the shorted diode does not allow any power produced by its panel to enter the system, thereby lowering system efficiency. Blocking diodes keep current from the battery pack, or a parallel panel string from entering a damaged string. This is important at night when the panel array cannot provide any power, thus providing a path for the battery to discharge. When installed, the blocking diodes may have leakage current on the order of nano- or micro-amps. However, if they fail due to ESD, they typically fail to a short circuit providing another path for the battery to discharge. This discharge current can be milli-amps or amps. (See Figure 3 for an example of this failure scenario.)

Failure of even one of these diodes in the field is very expensive for companies to replace due to the need for a qualified service technician, as most installations will require code requirements to be met. Continued operation of the panel array with a damaged bypass or blocking diode will, at best, hamper the array's efficiency and, at worst, cause permanent damage as it consumes power rather than produces power. It has been proposed that the damage to the diodes is caused by ESD stress.

What is ESD and how it damage the solar PV module diodes?

ESD is the sudden flow of electricity between two electrically charged objects caused by contact, an electrical short, or dielectric breakdown. Electrostatic discharge stress can occur in many forms and, depending on the characteristics of the stress, can damage different parts of solar PV module subjected to the stress. In particular, there are several ESD models with industrial standards that describe the pulse shape, source impedance, and determines levels at which the device should survive.

The commonly used ESD models (Table 1) are the Human-Metal Model (HMM) (IEC 61000-4-2 for system level ESD testing or ANSI/ESD SP5.6-2009 for component level ESD testing), the Human-Body Model (HBM) for component level ESD testing (ANSI/ESDA/JEDEC JS-001-2014), and the Charged-Device Model (CDM) for device level ESD testing (ANSI/ESDA/JEDEC JS-002-2014). There is also the Machine Model (MM), but it has been discontinued due to poor repeatability. Further, a new ESD model that currently has no established industrial standard, but has a different damage effect is the Cable Discharge Event (CDE).

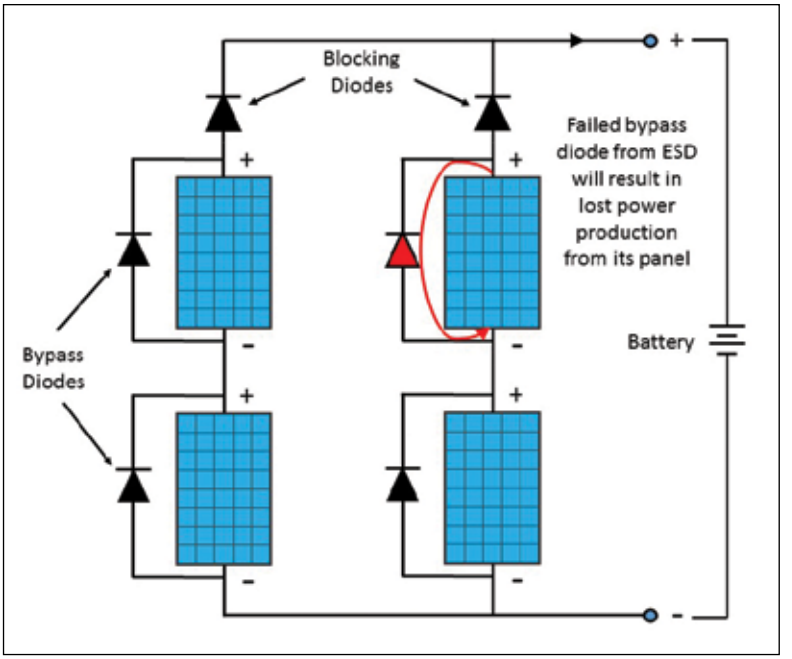


Figure 2: ESD damaged bypass diode fails short, disabling the PV module and lowering system efficiency

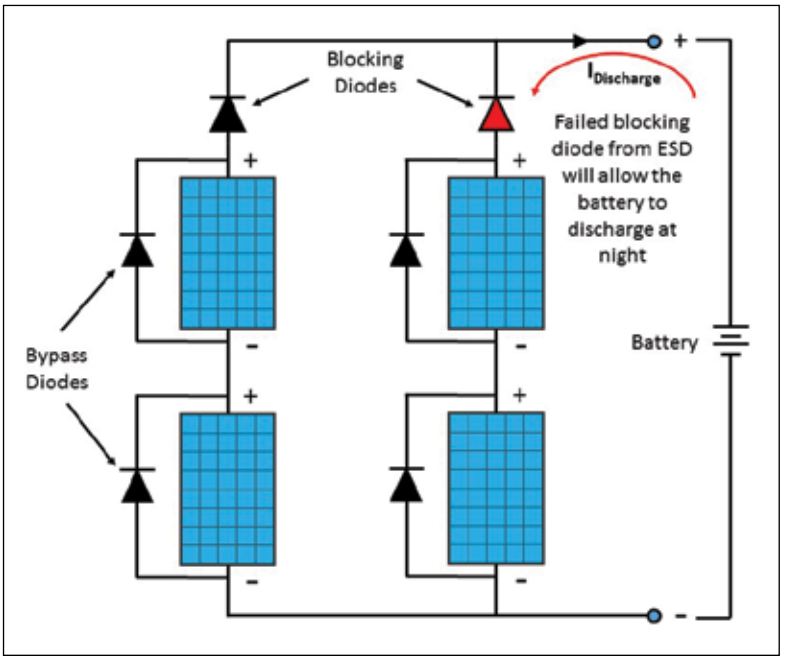


Figure 3: ESD damaged blocking diode fails short, allowing battery discharge path at night

ESD Model	Short	Applied DUT	Latest Industrial Standard	Comments
Human Metal Model	(HMM)	System level	IEC 61000-4-2 ED. 2.0 B:2008	Widely used standard
		Component level	ANSI/ESD SP5.6-2009	Pending to be a standard
Human Body Model	(HBM)	Component level	ANSI/ESDA/JEDEC JS-001-2014	Widely used standard
Charged Device Model	(CDM)	Device level	ANSI/ESDA/JEDEC JS-002-2014	Widely used standard
Machine Model	(MM)	Component level	ANSI/ESD STM5.2-2012	Discontinued
Transmission Line Pulse	(TLP)	Component level	ANSI/ESD STM5.5.1-2014	Widely used standard
Cable Discharge Event	(CDE)	System level	NA	Hard to be defined

Table 1: Widely used ESD models (as of September 2015)

Human Metal Model (HMM)

The human-metal ESD can take place when a charged person holding a pointed metal object, like a screwdriver or a ballpoint pen, rapidly moves the hand against an electronic device. In regard to PV module bypass and blocking diodes, this type of ESD events would most likely occur during junction box assembly with metal tools like tweezers, pliers, or screw drivers, etc. Figure 4 demonstrates a HMM event between a screwdriver and a screw that is part of an electrical installation in the junction box.

Human-Body Model (HBM)

Human-body model simulates the transfer of charge from a human to a component, such as through a fingertip as a device is picked up. This model is one of the most commonly used ESD tests for component qualification. In regard to PV module bypass and blocking diodes, this type of ESD event would also most likely occur during junction box assembly, especially if the operator picks a diode and mounts it by hand into the junction box. Figure 5 demonstrates a personnel picking up a PV module diode with bare fingers.

Figure 4: HMM event between a screwdriver and a screw that is part of an electrical installation in the junction box.

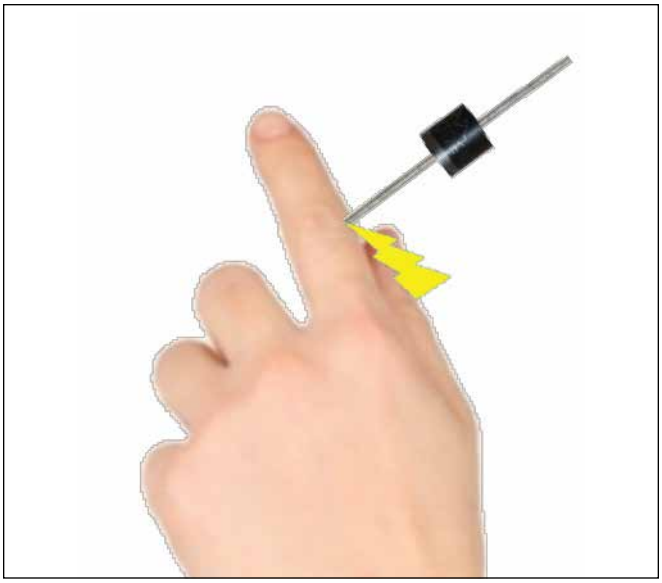


Figure 5: Potential ESD from HBM, picking up the diodes

Charged-Device Model (CDM)

Charged-device model simulates the transfer of charge from a device to ground. A device can collect charge by sliding across a surface and then discharged by contact to a metal surface or ground. In regard to PV module bypass and blocking diodes, this type of ESD event would most likely occur during junction box assembly.

Transmission Line Pulse (TLP)

The TLP technique is based on charging a transmission line to a pre-determined voltage, and discharging it into a device under test (DUT). The cable discharge emulates an ESD event that has better defined RF signal path, controllable rise-time, and pulse width. The test setup allows transient current and voltage waveform to be monitored. Therefore, the change of the DUT impedance can be monitored as a function of time in ps details. The DUT performance degrade or failure check can be automated with RF high voltage switch and help the system with faster ESD performance analysis. Regarding to the PV module diodes, this model is not a real-world event as the transmission line would not be well defined as the TLP model, but the type of waveform is relatively similar to cable discharge events (CDE) during the PV module on-site installation process.

Cable Discharge Event (CDE)

A cable discharge event is a frequent real-world electrostatic discharge event that occurs when a cable is connected onto a device and the cable has existing charge prior to making the connection. This can also happen by connecting a charged cable (open on one end) to a device. It occurs because there is a potential differential between the charge on the cable to be connected and the device. The resulting waveform is highly dependent on the real-world current return path and specifications of the cable.

However, these events usually have a fast rise time of less than 500ps, potential for high current that can reach over 100 Amperes, and a potential long pulse that can be several µs if the discharging cables are long. The fast rise time, high current, and long pulse duration can result in a permanent performance degrade or physical damage of device being subjected. Regarding to solar PV module, the cable connections between the panels can be very long, resulting the ESD current waveform could be very different from all previous cases. Because cable connection is an avoidable on-site installation process, cable discharge event should be treated as a special ESD case with special test setup for the PV module diodes quality assurance.

Although these ESD models describe how an ESD stress event may originate, the underlying physics of these models point to two basic damage causes. Damage may occur as the device cannot withstand the extremely fast voltage transient, or a device is not able to handle the current or the heating caused by the current. Here, the heating occurs within nanoseconds, such that there is no thermal exchange with the surrounding. Further, the current distribution within the conduction area of the device may not be homogeneous, such that local melting ("filament creation") leads to damage at current levels that the device could handle, if the current would flow with equal current density in the device.

The CDM model is used to qualify a device for the first of these damage types in that a very fast rise time as 100 ps with a short duration pulse. This test can determine if the gate oxide layer of a component is susceptible to a CDM type of event. The HBM model is used to qualify a device for the latter of the damage types in which a long duration (100ns) pulse is applied. The HMM, CDE and TLP models could possibly contain both types of damage. However, the CDE or TLP type of model would result in the worst possible damage in all of the cases discussed above.

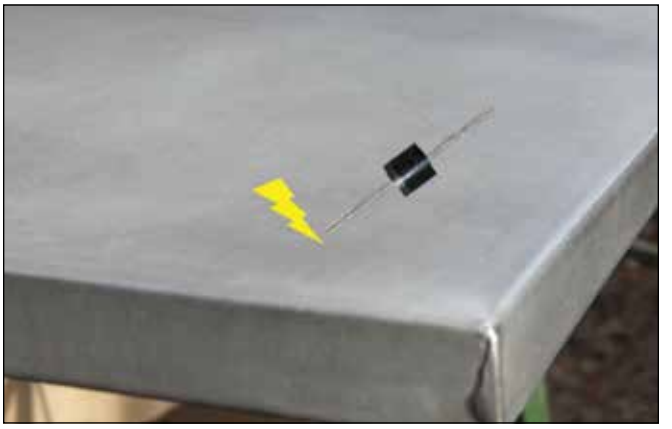


Figure 6: Solar PV module diode drops onto grounded metal surface

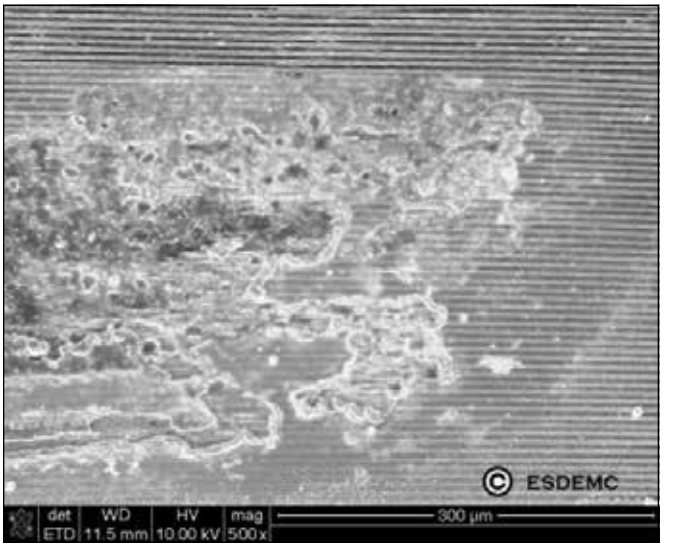


Figure 7: SEM image of die surface from ESD damaged PV bypass diode sample, melted metal and silicon observed.

Given the nature of how the bypass and blocking diodes could be exposed to and damaged by ESD events, the worst case that would be the cable discharge event, in which both fast rise-time and high energy pulses occur during the installation process.

An example of damage to the semiconductor components is shown in Figure 7 which illustrates burn track damage on a PV bypass diode caused by ESD.

THE TRANSMISSION LINE PULSE TEST METHODOLOGY

Given the nature of how the bypass and blocking diodes could be exposed to and damaged by ESD events, the worst case that would be the cable discharge event, in which both fast rise-time and high energy pulses occur during the installation process. Therefore, based on the existing industrial ESD testing methods, we propose to use the transmission line pulse test method that does not necessarily replace the IEC 61000-4-2 standard, which may have been be used in the current qualification process. Instead, the TLP test method subject a diode (a low resistance DUT) to a faster rise-time and higher energy pulse up to 180A (pulse reflections being allowed to approach the real-world CDE case). This provides a fully-automated device ESD performance characterization system for transient IV signal and degrade/failure inspection before and after each pulse. Compared to the other types of ESD models, the advantages of using a TLP test are:

- *Well Defined Consistent Waveform Shape:* Both circuit and waveform defined in ESD simulator standards are too flexible (no impedance control for test path, 30% tolerance at only certain time) This causes ESD simulators to provide very different ESD test results between different test sites. A TLP pulse is very clean and consistent.
- *Highly RepeaTable Test Setup:* Fatigue from holding ESD simulator by hand can lead to inconsistent test setups. In TLP testing with jigs for mounting the DUT, a more controlled test is obtained.
- *Fast Automatic Measurement and Reporting:* Typical TLP testing is done with full automatic control of oscilloscope scale adjustment, voltage pulsing, failure criteria checking, and IV curve update.
- *Important Device Behavior is recorded for ESD analysis and design:* Many useful parameters can be extracted from TLP tests for device transient behavior analysis, modeling and system-efficient ESD design (SEED). Traditional ESD tests only generate pulse for pass/fail results.

Test Setup

The TLP test setup is shown in Figure 8. A transmission line pulse (TLP) generator provides a rectangular voltage pulse by charging a 50Ω transmission line to a test voltage, and discharging the pulse to the DUT by a special relay which can withstand the voltage, and can switch to an on "on" status without bouncing. The pulse then travels out of the TLP through a coaxial transmission line where it first reaches a high voltage relay (A621-HVLKR).

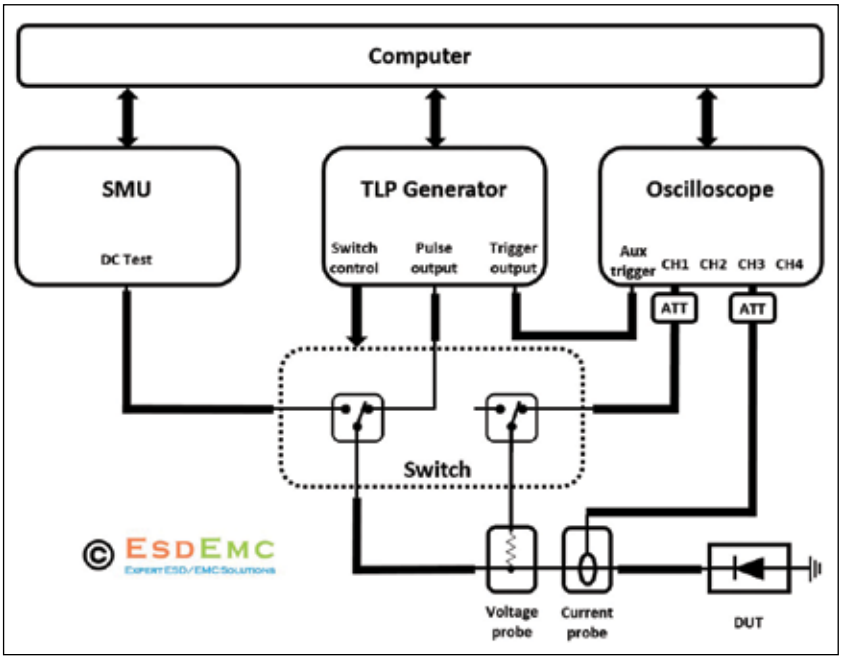


Figure 8: High current TLP test setup for solar PV module diodes

This relay is capable of withstanding up to 10kV, and is required for the high current TLP testing used with these high power diodes. The relay provides a means of transferring connection of the DUT between TLP measurement system and the failure detection system. In particular, during TLP pulsing, the relay connects the DUT to the TLP, the measurement probes, and the oscilloscope. After each TLP pulse test waveform has been captured, the system switches the DUT to the SMU to measure the diode reverse leakage current at maximum recurrent peak reverse voltage (VRRM). The A621-LTKSEM leakage test module also helps to facilitate these connection changes on the low voltage side of the measurement probes.

The DUT current is measured indirectly using a resistive tee to voltage measurement. The current is recovered by the overlapping reflection method. This method measures both the current through and the voltage across the DUT, but for low-resistance devices, such as a diode in the "on" state, this method is not well suited for measuring the device voltage. Instead, the DUT voltage is measured directly at the device, providing a highly accurate voltage probing measurement. The current measurement is performed by first measuring the pulse as it passes by the first pick-off resistor that goes to Ch1 of the oscilloscope. A short delay later (as determined by the length of coaxial cable between the pick off resistors), the pulse reflected from the DUT is measured at the same pick off resistor yielding an overlapped waveform. Using transmission line theory and a pre-measurement calibration pulse, the current into the DUT can be determined as:

$$IDUT = (V^{+} - V^{-})/Z_{o}$$

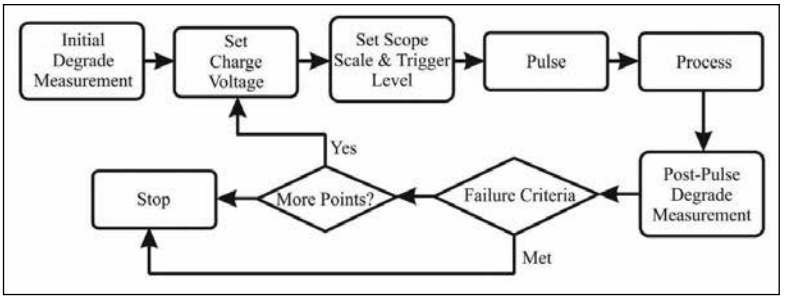


Figure 9: TLP test procedure flow chart

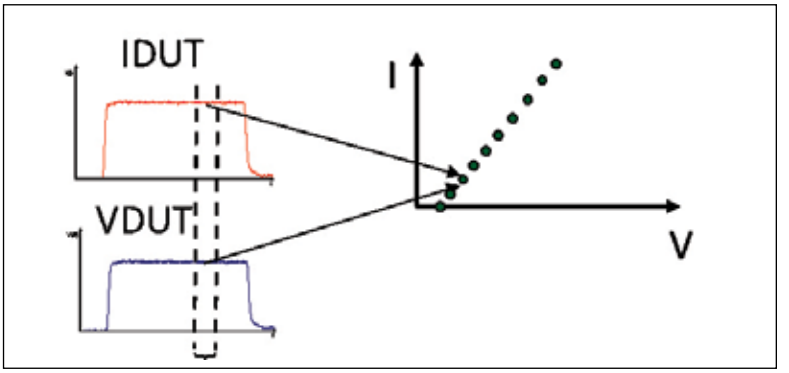


Figure 10: TLP test voltage and current waveforms during one pulse test

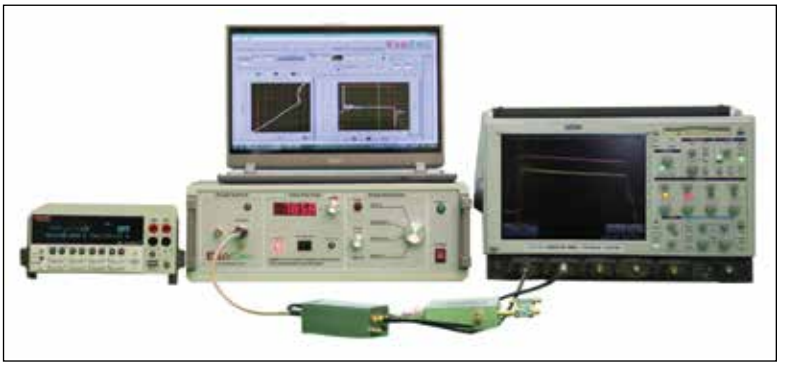


Figure 11: TLP System Setup

Equipment	Brand and Model	Specification and Comments
ESD Test	ES621-200 TLP System (A specially developed system, not a release model. The ES620-200 model may be released for a simplified turnkey solution)	<=1 ns rise-time, 100 ns pulse width, Max 10 kV charge line with no reflection rejection. The 10 kV charge voltage is achievable in the real world under dry conditions. The 100 ns pulse is represented approximately 10 meters of cable that is very close to the grounding conduit. Please note that during installation, a charged PV module connecting to a grounded cable will have the same effect as a charged cable discharging to a PV module. A 10 meter cable may not be the worst case since solar cables could be up to hundreds meters for certain systems.
Failure Test	Keithley Model 2400 or Keithley Model 6487	This configuration depends on the diode VRRM
Oscilloscope	LeCroy WaveMaster 8620A	6 GHz, 20 Gs/s (200 MHz min bandwidth per ANSI/ESD STM5.5.1-2014 standard)

Table 2: Solar PV module diodes TLP test equipment and settings

Upon entering the test loop, the system measures the leakage current of the DUT to obtain the initial degrade measurement. Next the TLP charge voltage is set. The charge voltage was set to sweep from 500V to 9600V, in 100V increments.

Where V^+, V^-, and Z_o are the incident pulse, reflected pulse, and characteristic impedance (50Ω) of the transmission line system, respectively.

Test Procedure

The test procedure is demonstrated in the flowchart shown in Figure 9. Upon entering the test loop, the system measures the leakage current of the DUT to obtain the initial degrade measurement. Next the TLP charge voltage is set. For the testing reported in this article, the charge voltage was set to sweep from 500V to 9600V, in 100V increments. For the first test point, the oscilloscope scale and trigger level are set based on the initial charge voltage and a 50Ω DUT. As testing progresses, the scale and trigger level are set based on if the waveforms clip, or is under scaled. If the waveforms do not clip or are not under scaled the settings are kept.

After setting the oscilloscope parameters, the DUT is pulsed and the captured data is compared to the oscilloscope display range for each captured channel to check for clipping and whether the scale is appropriate. If any of the waveforms are clipped, the scale is adjusted and the DUT is pulsed again. If the waveforms are ok, or under scaled, the data is accepted and processed. Any under scaled waveform corrections are made on the next pulse level. Processing is completed by scaling the data by the measurement attenuator and probe values.

Another DUT degrade/failure measurement (measure the PV diode leakage current under reverse working voltage) is made to determine if the DUT has failed or not. If failure occurs, the test is stopped. If. If not, the next pulse point is performed. This repeats until all pulse points are done, or failure occurs.

Dynamic IV Curve Measurement Principles

One of the goals of the measurement system described above is to obtain the dynamic IV curve of the DUT over the voltage range pulsed. Current and voltage waveforms resulting during pulse test are demonstrated in Figure 10. The dashed lines near the end of the pulses represent the start and stop points of the dynamic IV measurement window. The measurement window is typically 70 to 90% range of the pulse but other ranges can be selected. Over this window, the average value of the time waveform is taken as the current and voltage, respectively. This value is then plotted for each voltage pulse applied.

Degrade/Failure Measurement (Leakage Current Measurement)

The leakage current was measured using the source meter unit (SMU) and, depending on the diode tested, the bias voltage was varied between two and three different voltages with the maximum bias voltage set to the maximum recurrent peak reverse voltage (VRRM) for each diode. The VRRM voltage is listed in each individual diodes datasheet.

Diode Model	VRRM, [V]
Sample set #1	60
Sample set #2	50
Sample set #3	45
Sample set #4	40
Sample Set #5	150
Sample set #6	200

Table 3: Diode models tested and their VRRM

Also, for the results reported below, for any diode that failed the leakage current upper limit was set to 2.5mA (a value that is very high and can be treated as failure criteria). This is the compliance limit of the SMU and is not an indicator of diode characteristic after failure, other than they appear to fail to a short.

SOLAR PV MODULE DIODES TESTS

Over the years, ESDEMC Technology has tested several diode models for solar PV module companies. The VRRM (from device datasheet) of the diodes are listed in Table 3. The VRRM values are important because they provide the maximum bias voltage applied to the diode for leakage current measurement. This value is supplied by the device manufacturer, and is typically found in their respective datasheets.

In the following sections, the test results will be presented in terms of the best performer to the worst performer in regard to diode failure during TLP testing.

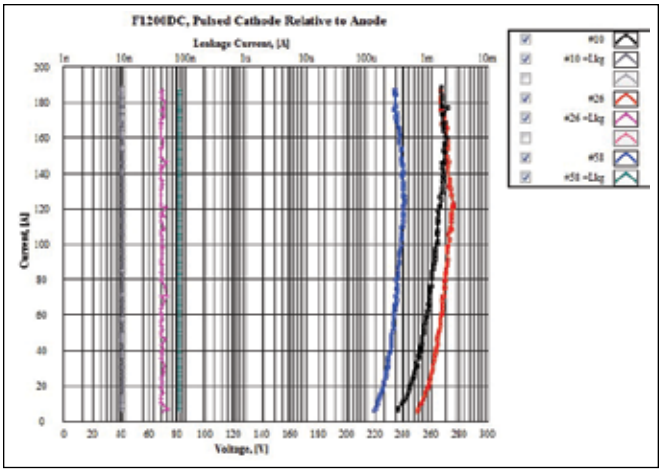


Figure 12: Sample Set #5, dynamic IV and leakage current @ high current TLP test

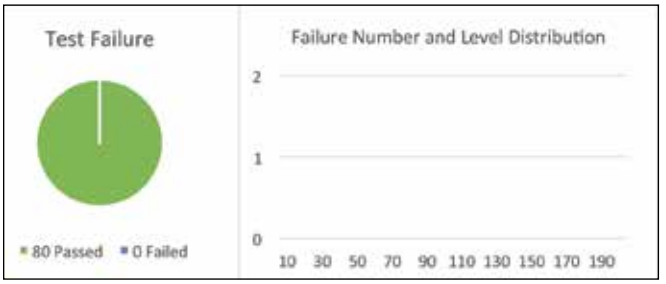


Figure 13: Sample Set #5, failure rate @ high current TLP test

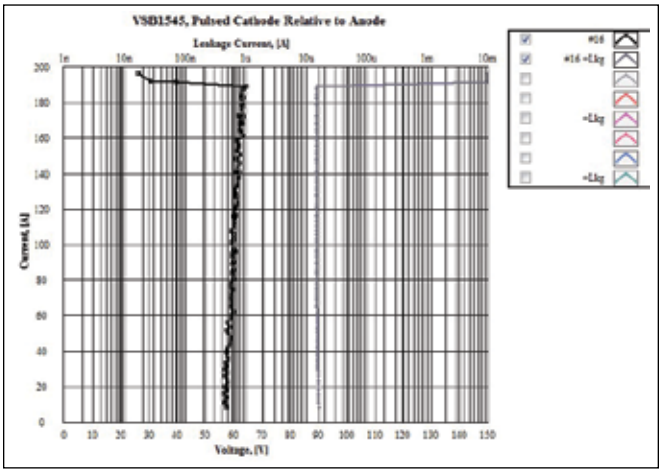


Figure 14: Sample Set #3, dynamic IV and leakage current @ high current TLP test

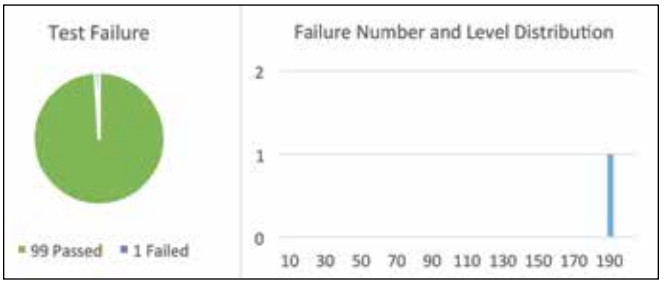


Figure 15: Sample Set #3, failure rate @ high current TLP test

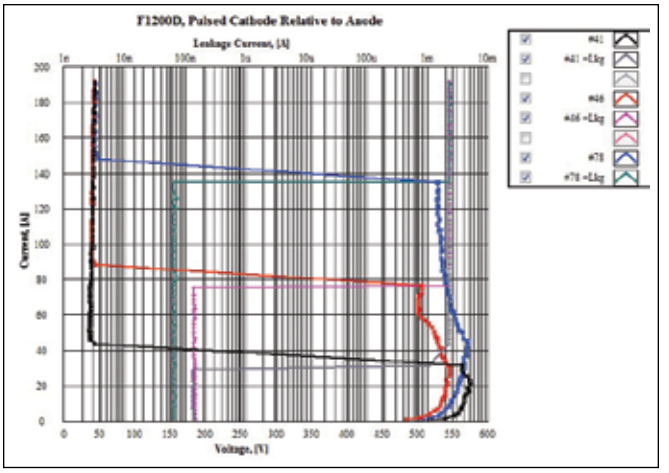


Figure 16: Sample Set #6, dynamic IV and leakage current @ high current TLP test

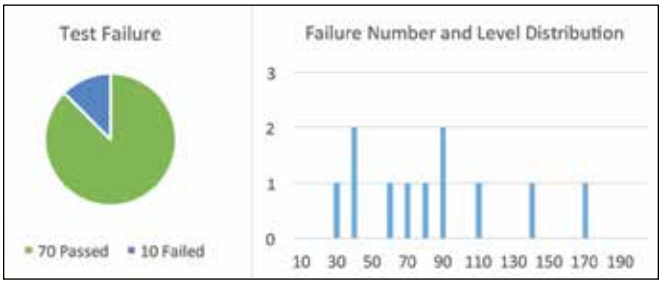


Figure 17: Sample Set #6, failure rate @ high current TLP test

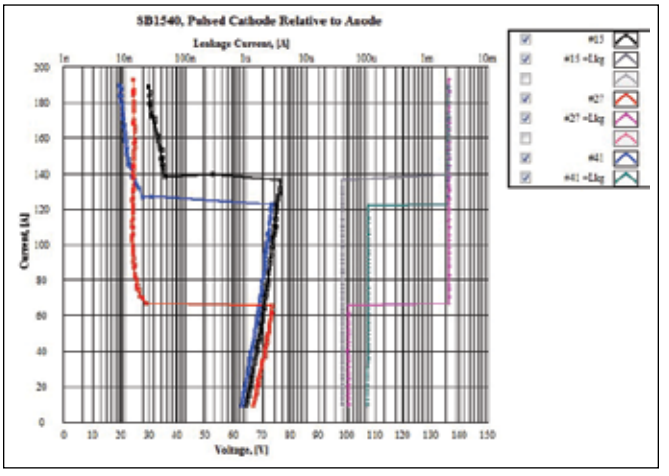


Figure 18: Sample Set #4, dynamic IV and leakage current @ high current TLP test

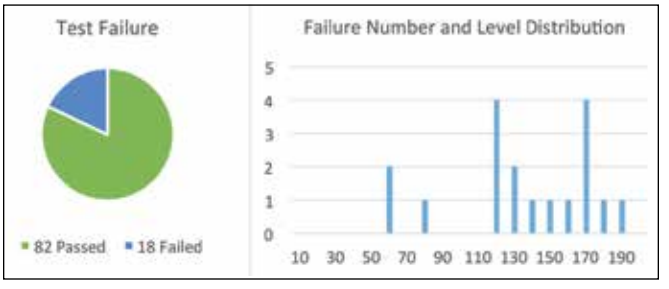


Figure 19: Sample Set #4, failure rate @ high current TLP test

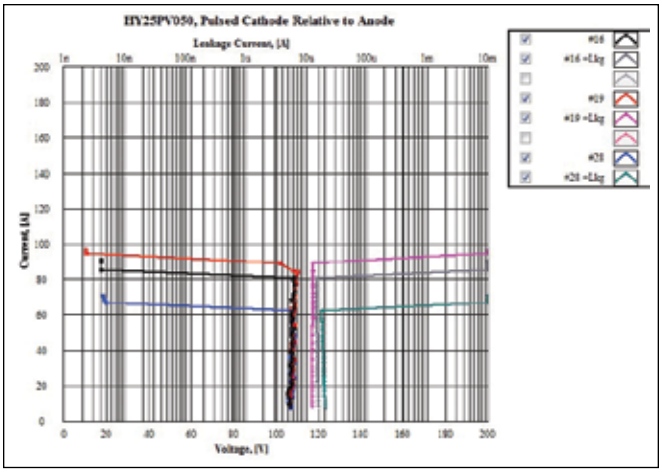


Figure 20: Sample Set #2, dynamic IV and leakage current

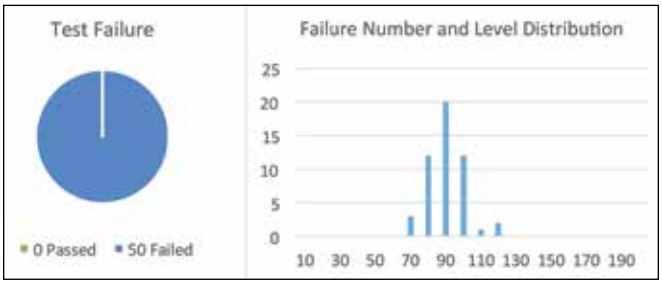


Figure 21: Sample Set #2, failure rate @ high current TLP test

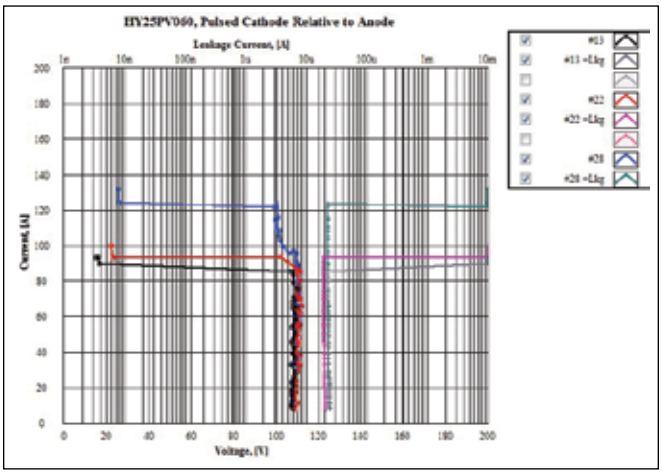


Figure 22: Sample Set #1, dynamic IV and leakage current@ high current TLP test

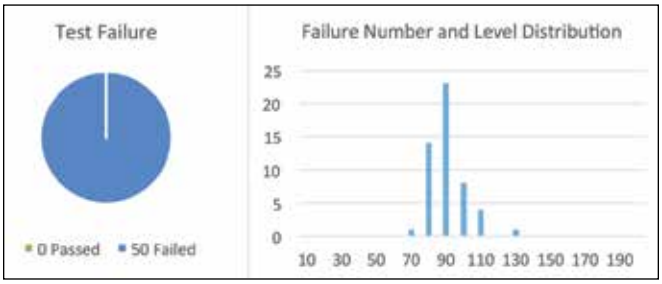


Figure 23: Sample Set #1, failure rate @ high current TLP test

Sample Set #5

Out of the 80 devices we tested in Sample Set #5, no failure occurred. The dynamic IV and leakage current curves for three samples are shown in Figure 12. The dynamic IV curve is read from the Y-axis to the bottom of the X-axis, and the leakage current from the Y-axis to the top of the X-axis. Note that the top of the X-axis is logarithmic due to the dramatic change in leakage current once a device fails to a short circuit.

Sample Set #3

The next best performers were the devices in Sample Set #3, which had only one diode fail out of one hundred units; failure occurring near the last few test pulse levels. The dynamic IV and leakage current curves are shown in Figure 14. Once the diode failed to a short, the resulting leakage current was at the compliance limit of the SMU, and is not an indicator of the diode condition.

Sample Set #6

Sample Set #6 had eleven failures out of eighty diodes tested. The minimum, maximum, and average pulse current for each of them are listed in Figure 25, and the dynamic IV and leakage current curves, for three of the failed diodes, are shown in Figure 16.

Sample Set #4

Sample Set #4 had 18 devices fail out of 100 tested. The dynamic IV and leakage current curves, for three of the failed diodes, are shown in Figure 18.

Sample Set #2

All of the diodes in Sample Set #2 failed. The minimum, maximum, and average pulse current for each of them are listed in Figure 25, and the dynamic IV and leakage current curves, for three of the failed diodes, are shown in Figure 20.

Sample Set #1

All of the diodes in Sample Set #1 failed. The minimum, maximum, and average pulse current for each of them are listed in Figure 25, and the dynamic IV and leakage current curves, for three of the failed diodes, are shown in Figure 22.

CONCLUSION

Of the diodes tested, only those in Sample Set #5 did not have failure up to 200 Amp or 10 kV of the eighty diodes tested. The next best performer was Sample Set #3, which only had only one failure, and that particular diode failed near the last few test pulses (100 diodes tested). Sample Set #6 had ten diodes fail out of eighty tested, and the Sample Set #4 had eighteen diodes fail out of one hundred tested. The worst performers were those in Sample Sets #1 and #2, where all diodes failed (all diodes tested failed for both models).

The chart shown in Figure 25 depicts the minimum, maximum, and average pulse current at failure for the diodes that failed.

It has been suggested that it is not necessarily the diode design type that determines if the diode is more or less susceptible to ESD stress, but instead a result of quality control of the manufacturing. For example, the process may be as follows: a diode as the 15SQ100 (tested data is now shown herein) is being checked in quality control after manufacturing. Its reverse breakdown voltage is checked. If it does not pass 100V, but passes 50V, it is re-labeled as a 15SQ050 model. This may not guarantee that the 15SQ50 model is a higher quality 050 design, and may instead be a poor quality 100 design relegated to the 050 model line. Here, the problem is that the diode may not hold 100V reverse voltage due to a local defect. The local defect will concentrate the current during ESD into a very small area and cause the diode locally to melt. Thus, the robustness of such a diode is much worse than a diode that passes the 100V reverse voltage, which may indicate that it does have few, and less severe local defects.

According to our customers (solar solution providers), our findings on the diode failure rate, through TLP test methodology, correlates to their field return failure rate. Therefore, we recommend that TLP testing be performed for all solar PV module diodes. In addition, it may be in the best interest of both solar PV module and diode manufacturers to investigate the quality control of the diodes selected, yielding a more reliable design for field use.

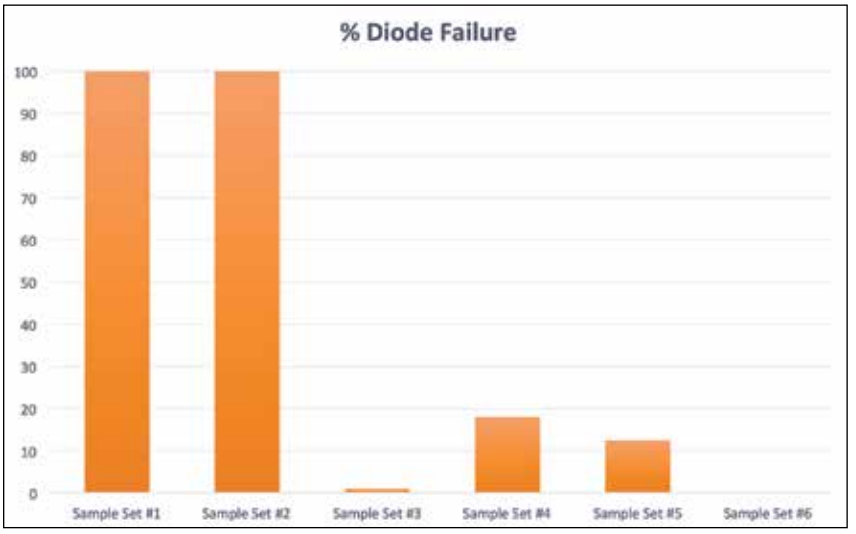


Figure 24: Diode failure rate comparison

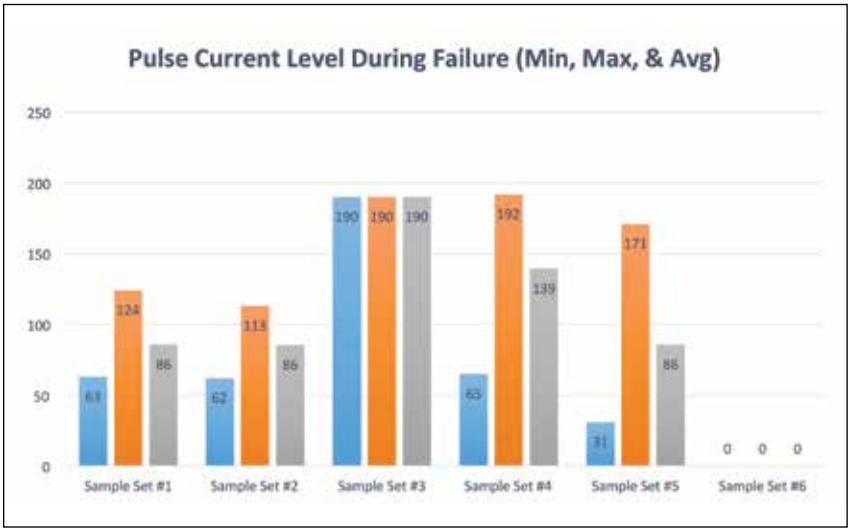


Figure 25: Minimum, maximum and average pulse current during failure for all tested diodes

REFERENCE

1. International PV Module Quality Assurance Forum, Task Force 4 (www.pvqat.org), Dec. 5-7, 2011.

Wei Huang *is the founder of ESDEMC Technology LLC and has been focusing on developing new ESD and EMC test solutions since 2011. Previously, he was a research assistant at the Missouri University of Science and Technology Electromagnetic Compatibility Laboratory with interests of electromagnetic, electrostatic and RF designs.*

Jerry Tichenor *is currently employed at ESDEMC as an Application and Design Engineer. Previously, he was employed at the Missouri University of Science and Technology as an Associate Research Engineer with interests of electromagnetic, renewable energy, and shielding effectiveness.*

David J Pommerenke *is a professor at the Missouri University of Science and Technology Electromagnetic Compatibility Laboratory. He has published more than 200 papers and is inventor on 13 patents. His main research interests are measurement/ instrumentation ESD and EMC.*