# An application of utilizing the system-efficient-ESD-design (SEED) concept to analyze an LED protection circuit of a cell phone

Tianqi Li [#1], Junji Maeshima [*2], Hideki Shumiya [*3], David J. Pommerenke [#4], Takashi Yamada [*5], Kenji Araki [*6],

[#] *EMC laboratory, Missouri University of Science and Technology, 4000 Enterprise Dr., Rolla, MO, 65401, USA*

[1] *tlx6f;* [4] *davidjp@mst.edu*

[*] *Sony Corporation, Sony City, 1-7-1 Kounan Minato-ku, Tokyo, 108-0075, Japan*

[2] *Junji.Maeshima;* [3] *Hideki.Shumiya;* [5] *TakashiB.Yamada;* [6] *Kenji.Araki@jp.sony.com*

***Abstract*—An LED circuit of a cell phone is analyzed using the System-Efficient-ESD-Design (SEED) methodology [1]. The method allows simulation of the ESD current path, and the interaction mechanisms between the clamp and the on-chip ESD protection circuit. The I-V curve and the non-linear behavior under high current pulses of every component including R, L, C, and ferrite beads are measured and modeled. By combining all of the component models, a complete circuit model is built for predicting the circuit behavior and damaging threshold at a given setting-voltage of a Transmission Line Pulser (TLP).**

## I. Introduction

To build lower cost systems with better ESD-resistant design at the system level it is important to understand the ESD current path, and how an IC's on-chip protection circuit interacts with outside clamp circuits [2]. For example, if the on-chip ESD circuit of an IO pin could provide enough protection, then any external protection components could be omitted to reduce cost. A more complex case would be if the on-chip ESD circuit could not meet the protection requirements and the off-chip protection circuit has a relatively large resistance, more ESD current would still flow through the IO pin's internal ESD circuit and finally damage the IO circuit itself. In this case, the external protection circuit should be replaced with a different clamp with smaller resistance in order to protect the IO pin.

For this reason, the interaction between components, especially between different protection circuits inside a system needs to be thoroughly analyzed, to achieve a more efficient protection scheme at the system level [1]. This is the purpose of the SEED approach. Circuit modelling and simulation is a convenient approach for such SEED analysis. However, typical SPICE models of components cannot be used in these simulations because they usually only contain information for normal operating conditions, without responses to several kV pulses such as those seen in ESD strikes. In this project a TLP is used to measure transient I-V characteristics of each component, and high-voltage-SPICE models are built based on the tested data [3].

In this paper, an LED circuit in a cell phone is chosen to demonstrate the SEED analysis approach. The schematic of the LED circuit is shown in Fig.1. Under typical working conditions the VCC pin outputs DC current that flows through the LED and is sunk by the IO pin. The driver IC controls LED turn-on and turn-off by changing the status of the output MOSFET. All other components such as capacitors and Zener diodes are used for ESD protection and other filtering purposes. A potential discharge point is at the LED, which is located near the cell phone's keyboard.

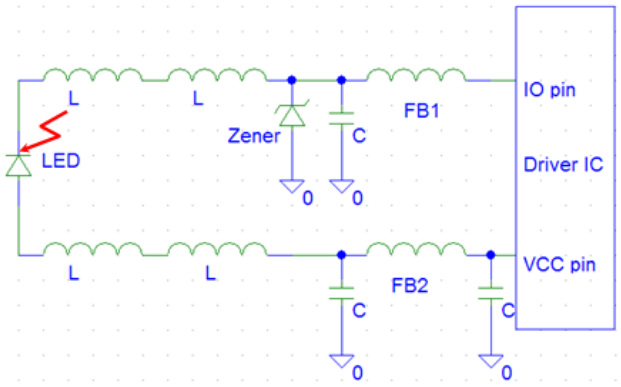


Fig. 1. Schematic of a cell phone's LED circuit under SEED analysis

## II. Components Characterization and Modeling

### A. Modeling the LED

The I-V curve of the LED has been measured using a TLP resulting in the SPICE model shown in Fig. 2. The model includes two parts: the normal-condition SPICE model which is provided by the device manufacturer, as well as switches for matching the transient I-V curve. The factory model is OK for emulating the device I-V curve in the positive voltage region, but does not conform to the I-V curve in the negative-voltage region. For this reason, two switches are used to correct the simulated I-V curve.

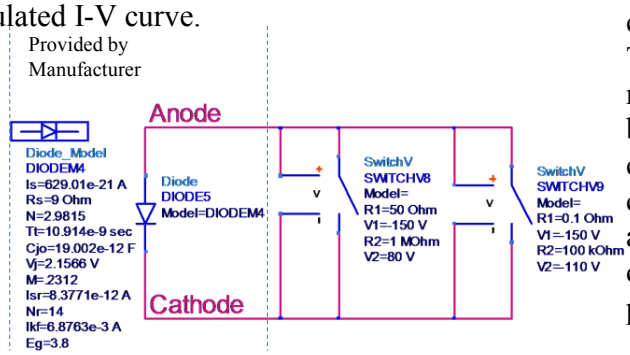


Fig. 2. The high-voltage-SPICE-model of the LED

From the simulation result which is shown in Fig. 3, it is clear that the model conforms well to the measured I-V curve.

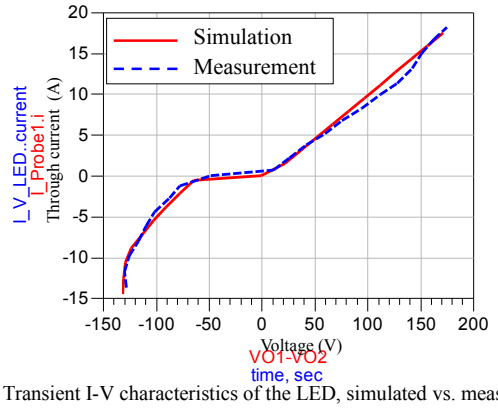


Fig. 3. Transient I-V characteristics of the LED, simulated vs. measured

During the measurements, it was also found that the LED will be damaged if the current reaches +15A or -10A.

### B. Modeling the Zener Diode

The Zener diode was modeled in a similar way. In the model which is shown in Fig. 4, diode 11 defines the I-V characteristics of the Zener under a negative pulse. Diode 10 and the switch determine the positive I-V characteristics. Diode 9 is used as a unidirectional switch.

A linear capacitance of 25 pF is also included. Its value is taken from the datasheet and verified through measurements.

The simulation results of this model (Fig. 5) show good agreement to measurements as well.

### C. Modeling the IO Pin of the LED Driver IC

A reflection-based TLP system is used for in-system measurement of the transient I-V curve of the IO pin, which is modeled without knowledge of its internal circuit. Similarly, the model is a combination of linear and non-linear components. The non-linear behavior was measured by the reflection-based TLP system, and its linear part can be obtained by tuning the model parameters to conform to the measured S11. In this way, a complete model of the IO pin could be developed, as shown in the Fig. 6. R20 and C2 are these linear components which were obtained from the S-parameter measurement.

Similar to the Zener diode model, diode 7 defines the non-linear behavior of the device when a negative pulse is applied at the IO pin. Diodes 6 and 8 define the non-linear behavior when a positive pulse is applied to the IO pin.

Fig. 4. The high-voltage-SPICE-model of the Zener diode

A damage threshold of 22A was determined using a 13.5 ns pulse from the TLP to the IO pin. The transient I-V curve of the model is shown in Fig. 7.

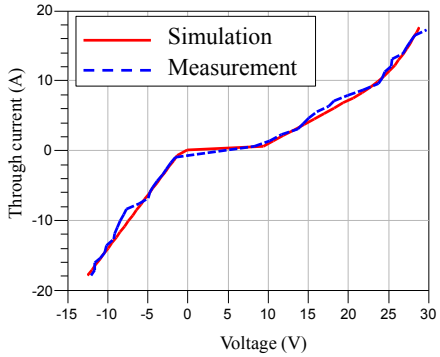


Fig. 5. Transient I-V characteristics of the Zener diode, simulated vs. measured

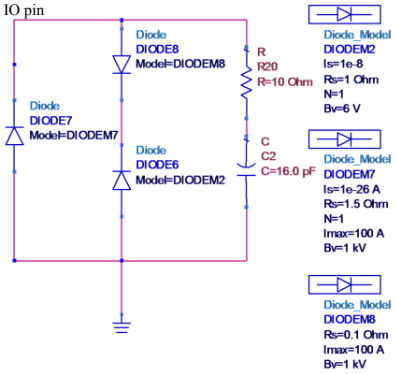


Fig. 6. Model of the IO pin of the LED driver IC

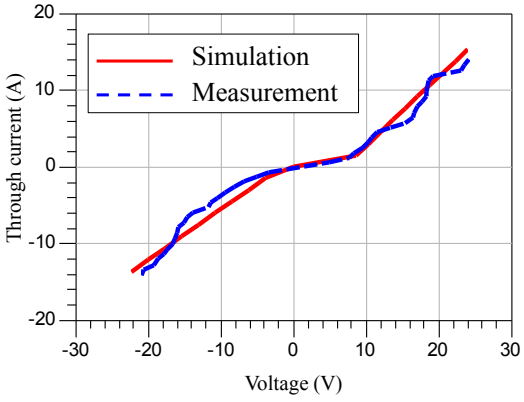


Fig. 7. Transient I-V characteristics of the IO pin, simulated vs. measured

*D. Modeling the Ferrite Beads*

Because ferrites are non-linear components, their equivalent inductances drop as through currents increasing, due to saturation effect. A non-linear model of the ferrite bead, as shown in Fig. 8, was obtained by defining its equivalent inductance as a function of current.

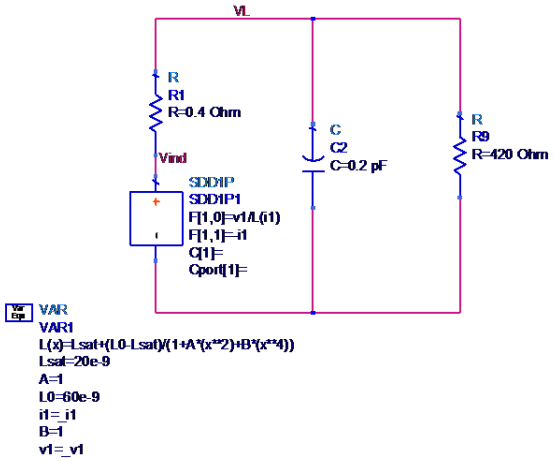


Fig. 8. Non-linear model of the ferrite bead FB1

In this model, the linear parts include R1, C2 and R9, which are extracted from the impedance plot provided by the datasheet.

The non-linear part of the ferrite model, the inductance as a function of current, was measured by a TLP, and modeled with following equation:

$$L(I) = L_{sat} + \frac{L_0 - L_{sat}}{1 + I^2 + I^4} \qquad (1)$$

Where I stands for the current through the non-linear inductor, $L_0$ is the inductance value for I=0. Thus, for FB1 $L_0$ equals to 60nH. $L_{sat}$ stands for the saturated inductance which, for FB1, equals 20nH. The plot of the equation is shown in Fig. 9.

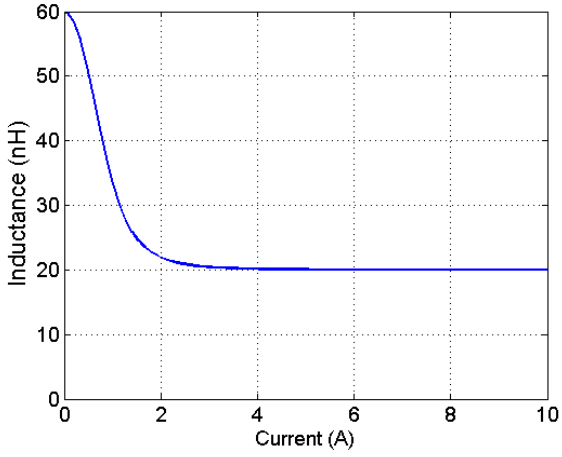


Fig. 9. Inductance as a function of current defined with the equation (1)

The model is validated by comparing simulation and measurement results, as shown in Fig. 10, the

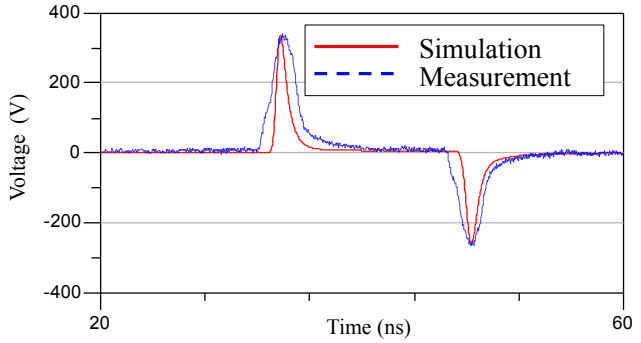


Fig. 10. Ferrite bead FB1's transient response under a 1050V TLP pulse in the reflection-TLP system, simulated vs. measured

### *E. Modeling the Inductors*

The inductors used in the circuit are assumed to be linear components, and the transient simulation result, as shown in Fig. 11, validates this assumption.

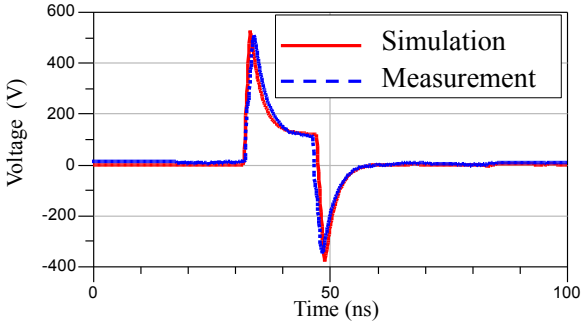


Fig. 11. The inductor's response under 1050V TLP pulse in the reflection-TLP system, simulated vs. measured

### *F. Modeling the Capacitors*

The capacitors used in this circuit have anNP0 type dielectric, therefore it was expected that the capacitance would not change as a function of the voltage across the capacitor. Such expectation was validated by measuring capacitance variation with respect to voltage by using a TLP. These TLP measurements confirm that the NP0-dielectric capacitor can be modeled as a simple linear capacitor.

## III. System Model and SEED Analysis

### *A. The System Model*

A system model was built by combining each of the experimentally obtained component models, as well as a TLP model as the source. The system model is validated through S-parameter measurements, as well as transient pulse measurements. The simulation result is compared to the measurement in Fig. 12. This comparison clearly shows that the injected 500 V TLP pulse is clamped to 9V by the protection circuit.

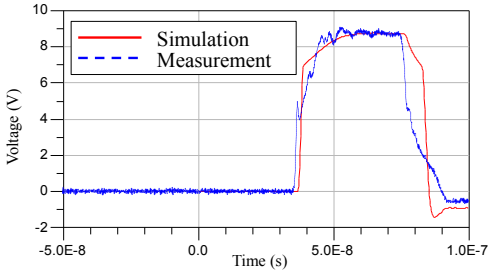


Fig. 12. Circuit response measured at the IO pin due to a 500V TLP pulse injection at the anode of the LED, simulation vs. measurement

### *B. SEED Analysis*

From Fig. 12, although it is known that the injected pulse is clamped to a low voltage, it is not known which one of the clamp circuit components is the primary clamping element. Additionally, it is not easy to predict what level of the injection pulse will damage the circuit, due to the fact that only a limited number of DUTs were available for real testing.

With the SEED method, the previous questions can easily be answered because it is possible to observe currents as they flow through various components in a simulation environment. In Fig. 13, it is clearly shown that more pulse current flows though the Zener diode during the first 10ns of an applied pulse before the protection diode inside the IO pin starts to conduct.

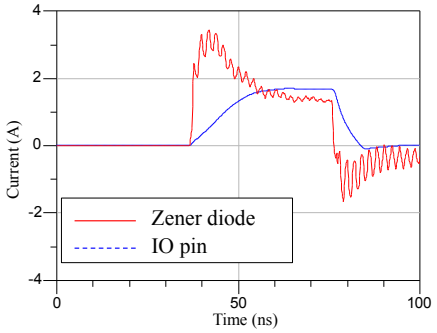


Fig. 13. Simulated IO pin current and Zener diode current when a 500V TLP pulse applied at the anode of the LED

If the Zener diode is a more effective form of ESD protection we can ask if it is possible to remove FB1 before the IO pin to reduce cost. The simulation result in Fig. 14 shows that without the ferrite bead more current would flow through the

IO pin, but not the Zener diode. Therefore, the ferrite bead has significant effect on the current that flows through the IO pin, and thus should not be removed.

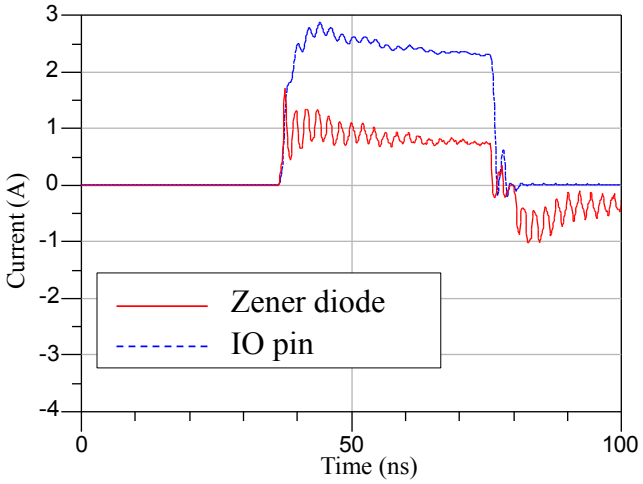


Fig. 14. Simulated IO pin current and Zener diode current when a 500V TLP pulse applied at the anode of the LED, and FB1 is removed

SEED analysis may also tell us what the vulnerable parts in this circuit are, and how much margin left till the circuit would fail under a given injecting level, if the damage threshold of each component is known. For example, the simulation result in Fig. 15, shows that the current which flows though the LED is much larger than the current that flows through the IO pin. Therefore, for this circuit, the LED is more prone to damage than the driver IC, especially considering that LED device is usually placed at a location that has a greater chance to experience air discharge. It can be predicted that the LED will be damaged under 2000V TLP pulse because under this condition the LED's through current reaches to 15A, which is its damaging threshold measured with 13.5ns TLP pulses.

## IV. Conclusion

In this study, the SEED strategy is applied to analyze the ESD performance of a cell phone's LED circuit. High current SPICE behavioral models of each component in the circuit were developed and validated against measurements. By combining these models with a TLP source model, major pulse-current paths, protection mechanisms, system transient response, and weak points of the protection circuit are revealed. These parameters can then easily be analyzed through simulation, instead of performing a large number of destructive measurements.

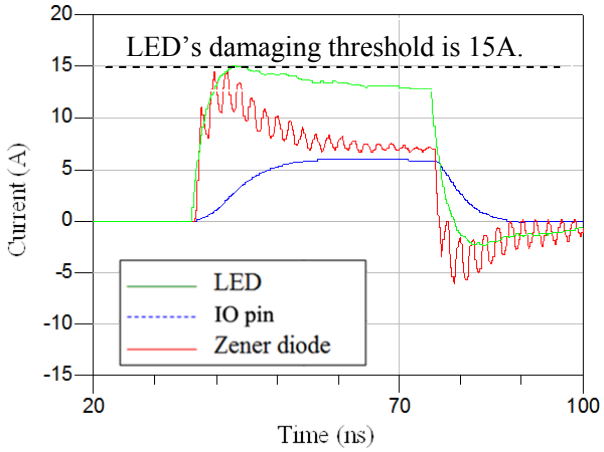


Fig. 15. Currents of LED, driver IC's IO pin and Zener diode when a 2000V TLP pulse applied, simulated by ADS

For next step, the TLP model can be replaced with an ESD gun SPICE model, so that we can predict the circuit's response under real ESD gun contact discharge measurements. This may help circuit designers predict the ESD performance of a circuit before it is put in to production. This SEED strategy also facilities PCB level ESD protection design during initial product development, rather than traditional trial-and-error process.

## Acknowledgment

This material is based upon work supported by the National Science Foundation under Grant No. 0855878, and supported by Sony Corporation of Japan.

## References

[1] Industry Council on ESD Target Levels, "White Paper 3, part 1," 2010.
[2] Harald Gossner, Werner Simbürger, M. Stecher. System ESD robustness by co-design of on-chip and on-board protection measures. *Microelectronics Reliability*, 2010: 1359~1366
[3] T.Maloney and N.Khurana, "Transmission Line Pulsing for Circuit Modeling of ESD Phenomena," in *Proc. On EOS/ESD Symp.*, pp. 49-54, 1985
[4] Johnsson, D.; Gossner, H.; , "Study of system ESD codesign of a realistic mobile board," *Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), 2011 33rd NO POD PERMISSION , vol., no.*, pp.1-10, 11-16 Sept. 2011
[5] Lifang Lou; Duvvury, C.; Jahanzeb, A.; Jae Park; , "SPICE simulation methodology for system level ESD design," *Electrical Overstress/ Electrostatic Discharge Symposium (EOS/ESD), 2010 32nd , vol., no.*, pp.1-10, 3-8 Oct. 2010