Measurement Methodology for Field-Coupled Soft Errors Induced By Electrostatic Discharge

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Abstract—High-speed low-power mobile devices are sensitive to electrostatic discharge (ESD)-induced soft errors, such as unwanted reset, lock up, loss of user interface, disturbed displays, etc. ESD can couple via current and fields into the internal cabling, printed circuit board traces but also directly into the integrated circuits (ICs). Many portable devices shield nearly all traces using top and bottom layer ground planes, and they apply effective filters at cable entry points such that direct field coupling to the IC can dominate the system’s ESD sensitivity. However, a little information is available on the robustness of ICs against direct ESD transient field coupling. A methodology for determining this robustness was developed and applied to a set of consumer electronic ICs to create an initial robustness database. Custom-made electric and magnetic field probes are driven by a 400-ps rise time transmission line pulse to evaluate 37 different ICs. The investigation showed that 50% of the ICs were disturbed at approximately 33 kV/m for the electric field injection and 142 A/m for the magnetic field injection at this rise time. This methodology can serve as the basis for further investigations of ICs. The database can be used to estimate the likelihood of field-coupled ESD-induced soft errors in electronic products.

Index Terms—Database, electrical static discharge, field-injection probes, integrated circuits soft error.

I. INTRODUCTION

OFTEN, the designers of electronic products face the problem of soft errors caused by electrostatic discharge (ESD). This can be not only caused by the discharge current, but also from transient electromagnetic fields [1], [2]. When a system is exposed to an ESD, a strong electromagnetic field can couple through apertures, cables, or slots into the enclosure [3], [4]. The induced voltages, impressed currents, and direct field coupling can disturb the operation of the integrated circuits (ICs); e.g., it can cause bit errors, fast transient latch up, etc. The ESD induced errors generally manifest as stripes on LCD displays, blackout errors, system hang, or system reset. Most of the errors are transient in nature and are cleared automatically, but some errors may require user interaction to reset the device to its normal working state.

Soft-error models are needed to determine if the simulated field strengths will lead to a disturbance. Sensitivity data from system-level ESD testing [5], [6] and from testing of PCBs with attached wires is available in the literature [9], [10], but disturbance thresholds for ESD induced fields for individual ICs have not been published, to the best of the authors’ knowledge. Full-wave simulation of a complete product, including ICs and PCB details, is not currently possible because of the complexity of the structures, the lack of soft-error models for ICs, and the proprietary nature of information from multiple vendors. The characterization methodology and database presented in this paper will serve as an initial step toward allowing a preliminary judgment of the likelihood of a field-coupled disturbance. This three-step assessment process involves: 1) a simplified full-wave block level simulation [7], [8] that provides the field strengths inside the product, then 2) that information is translated by the database into the likelihood of a soft-error occurrence, and then 3) if the database indicates a high likelihood of disturbances, either the system design can be modified to reduce the field strengths or the specific ICs used in the system can be characterized using the field injection method explained in this paper. Not every IC can be tested for its field coupling sensitivity, so a statistical approach was utilized to predict the approximate soft-error levels. The novelty of the research lies in the creation of a database for a wide variety of consumer electronics ICs, as well as in the test methodology. The results are based on the evaluation of 37 ICs: as more products are tested, the database will be extended in future publications.

Many portable electronic products, such as cell phones, have hardly any surface traces because the PCBs are densely filled with components and ground planes. Furthermore, stacking PCBs and other metallic structures, such as a battery in close proximity to a PCB, greatly enhance the transient field strengths during an ESD if the discharge injects current into, for example, the battery, and there is an inductive connection to the PCB. Because of the lack of global shielding in many consumer electronic products, ESD discharges can cause transient fields large enough to disturb the ICs by direct field coupling [11]. Direct coupling is quite common in consumer electronics, so this database focuses on direct field disturbances. These transient field levels are usually large and cannot be reached during tests applying modulated sine wave signals, such as the radiated immunity test (IEC61000-4-3) [12]. Pulsed high-power microwave testing and especially ESD testing (IEC 61000-4-2) [13] can reach field strengths high enough to cause direct field-coupled soft errors. As this study focuses on the immunity of consumer electronic products to ESD, only ESD-like pulses were used.

Field coupling to ICs usually is achieved by either transverse electromagnetic (TEM) field methods or near-field scanning [14]. The TEM fields usually are achieved by either transverse electromagnetic (TEM) field methods or near-field scanning [14].
Fig. 1. Test set up for measuring the induced voltage caused by the electric field.

TEM cell [15] or other TEM wave guiding structure, such as the IC stripline [16]–[18]. To focus the coupling onto a single IC, this test method requires a special test board [17]. Furthermore, when using a TEM cell, it is not possible to distinguish directly between electrical field and magnetic field coupling. Many TEM cell structures allow the propagation of higher order modes above 1 GHz [19]. Only the newly developed smaller structures prevent higher order modes up to a few gigahertz, which is sufficient for ESD field testing if a test board is available. Near-field probes placed directly upon the IC overcome these limitations.

Details of the probe design and calibration appear in Sections II and III, respectively. Section IV focuses on the soft-error testing methodology, and Section V is devoted to the presentation and analysis of the database results.

II. HARDWARE DESIGN

A. Electrical Field Probe

The probes must cover the entire top surface of the IC under test to illuminate them with a relatively homogenous field distribution. Furthermore, they must be able to withstand 8 kV from the transmission line pulser (TLP) used as the source [20]–[22].

A square copper patch created the electric field. To avoid ringing caused by the probe’s coax cable and to couple the probe’s local ground via displacement currents to the PCB ground, a larger disk made from lossy conductive material was attached to the coax cable shield. The lossy disk offered a termination for the high-frequency spectral content flowing on the outside of the coax cable shield, which helped to create a clean pulse.

The drawing of the E-field probe and its calibration measurement setup is shown in Fig. 1. A TLP having a pulse width of approximately 10 ns and a rise time of 400 ps was used to rapidly charge the probe as shown in Fig. 2. The field strength is directly proportional to the charge voltage. The probe was placed close to a patch situated on a PCB. A two-layer PCB with a patch having the same dimensions as the probe captured the transient fields created by the probe as shown in Fig. 3. The patch was terminated with 50 Ω. The probe induced a voltage on the patch that peaked at approximately 190 V when the output voltage of the TLP was set at 500 V. A small amount of ringing was visible, and the pulse rose in approximately 200 ps.

B. Magnetic Field Probe

The design goals for the magnetic field probe were similar to those of the electric field probe. The probe should produce a nearly uniform magnetic field over the surface of the IC over a frequency range of up to a few gigahertz. Also, the electric field produced by the probe should be minimized. Previously designed magnetic field probes were hampered by either an insufficient area for the magnetic field coupling or an insufficient homogeneous magnetic field within the desired coupling area.

Figs. 4 and 5 depict the design principle and the performance data. The magnetic field probes were designed to have different sizes, using four-layer PCBs, to match the sizes of the different ICs. No linear relationship exists between the field strength and the probe size. To determine the field uniformity, an S21 measurement was performed by receiving the field produced by the probe on terminated microstrip traces fabricated on a PCB.
Fig. 5. Contour plot of S21 magnitude measured at different points underneath the probe at 1 GHz, 0.5 mm below the probe surface. The active area of the sensor is indicated by the dotted line. The field strength is relatively constant within this region which covers the ICs tested.

Fig. 6. Full-wave model of the E-field probe with lossy disk. The common mode return current is modeled by a semicycle wire which represents the coax cable connection.

The magnetic field probe was moved to inject over an array of 400 points evenly distributed over the PCB. The resulting S21 distribution appears in Fig. 5. The orange trapezoid represents the sensor area. The variation of the field was within 2 dB underneath the center sensor area.

III. Probe Calibration

A. E-Field Probe Calibration

A full-wave model of the E-field probe shown in Fig. 6 was created to determine the conversion factor between the TLP voltage and the electric field strength underneath the E-field probe. Similar to the calibration performed in measurement, the simulation model placed a 50-Ω loaded patch underneath the probe and simulated the induced voltage. The probe provided approximately 50 kV/m at a TLP setting of 1 kV as shown in Fig. 7. This resulted in a calibration factor of 50 V/m per volt. The observation point was set at 2 mm below the center of the E-field probe, which approximated a typical distance between the die of an IC and the probe’s metallic structure. The probe’s performance was experimentally validated.

B. H-Field Probe Calibration

Calibration of the H-field probe is a two-step process. First, a reference probe was calibrated by inserting it into a standard TEM cell using a VNA. This allowed the probe factor and the effective loop area of the reference probe to be determined. Then, the reference probe was used to measure the field strength of individual magnetic field probes driven by a TLP [23].

For calibrating the reference probe, a 10 × 10 cm² board with a slot was used to cover the top wall of the TEM cell, and the probe was inserted into the cell through the slot as shown in Fig. 8. Using Faraday’s law, the measured response as captured by a VNA can be given as

\[ v_2 = A_{\text{eff}} \mu \frac{dH}{dt} \] (1)

where \( v_2 \) is the measured response on port 2, \( A_{\text{eff}} \) is the effective loop area, and \( \mu \) is the magnetic permeability of free space. Using the free-space impedance relation

\[ H = \frac{E}{377} \] (2)

the electric field strength can be approximated in terms of the input excitation inside the TEM cell as

\[ E = \frac{v_1}{h} \] (3)

where \( h \) is the height between the probe and the septum of the TEM cell which is approximately 45 mm and \( v_1 \) is the input excitation. The frequency response of the reference probe increased with a slope of 20 dB/dec up to and beyond 600 MHz. Using (1)–(3), the effective loop area of the reference probe was
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Fig. 9. Effective area approximated from measurement. The drop above 600 MHz is caused by the beginning influence of self-integration due to the self-inductance and the load impedance. The method of calculating the effective area does not take this into account; thus, a deviation from the 20 dB/dec increase is expressed as a reduced effective loop area.

Fig. 10. Measurement setup to measure the field strength of H-field probes, using a reference probe with a known effective area.

approximated from measurements to be 1.6 mm² as shown in Fig. 9.

After determining the probe factor of the reference probe, the reference probe was used to measure the field below the H-field injection probes. Fig. 10 depicts the measurement setup. The measured voltage was converted to the magnetic field using

$$H = \int \frac{V}{A_{\text{eff}}} \, dt$$

(4)

where $V$ is the voltage measured by an oscilloscope in the setup shown in Fig. 10. Normalizing the measurements to 1-V TLP charge voltage led to field strengths of 0.15 to 0.2 A/m/V depending on the size of the H-field injection probe.

IV. TEST METHODS FOR DETERMINING THE SOFT-ERROR THRESHOLDS

A. IC Selection Method

All IC selection methods bias the database. Our objective was to create a database for high-volume consumer electronic products. Physically small ICs, such as power supply controllers, simple logic circuits, and motor drivers, were not selected because prior experience in ESD near-field scanning [24]–[27] has shown that those types of ICs are usually robust against field coupled ESD pulses. Instead, we selected the highly complex VLSI ICs as field injection targets. Typically ICs selected for this testing were multifunctional ICs, microcontrollers, and DSP chips.

Examples of products selected for this analysis include cell phones, USB hubs, MP3 players, Ethernet switches, desktop LAN switches, DVD players, webcams, digital photo frames, wireless routers, and digital SLR cameras.

Every observable behavior change in the normal functioning of the product as a result of E-field or H-field injections was considered a soft error. Observed soft errors included system resets, interruption of playback, changes in LCD displays, inability to control the system through its user interface, abnormal termination of USB data transfer, etc.

B. Measurement Set Up

A total of 37 ICs were tested. It was not possible to conduct every test on every IC. Limited space around some ICs prevented testing them with both types of probes. In other cases, the product was damaged before testing was completed. Fig. 11 illustrates the measurement setup on an example IC. During the test, the injection probe was placed onto the subject IC while the device was on. TLP pulsing was applied at approximately 10 pulses/s. The charge voltage was increased gradually until either a soft error was observed or the maximal charge voltage of 8 kV was reached. Fig. 13 displays a photo of an error captured during the testing of a digital photo frame.

In addition to direct probe placement testing, a 1.2-mm FR4 spacer was added between the test ICs and the field injection probes to investigate the effect of increasing the distance between the probe and the IC. Fig. 12 illustrates the stack up for E-field injection.

The spacer was used to determine the consistency of the database, as the observed change in the soft-error threshold should match the field strength reduction caused by the spacer. Furthermore, a 100-MHz high-voltage low-pass filter was added
before providing the pulse to the probe. The low-pass filter removed high-frequency content, allowing the soft-error threshold for different spectral content to be recorded.

V. RESULTS OF THE DATABASE

A. Data Analysis

To process data from different test configurations performed on the same IC, the following method was selected. For every test, a “virtual” IC was created in the database. There were differences in the field sensitivity results when using different probes because of the effect of other field components on the probes, especially at the edge, as well as possible mismatches between the probe and IC size, and calibration inaccuracies. The average difference was within 20% for E-field results and 10% for H-field results. We included both results in the database; thus, again creating two data points for the E-field and two for the H-field for each IC.

Magnetic field coupling results were obtained for two perpendicular placement orientations on the IC, but only the result from the more sensitive orientation was included in the database. The database also includes results from both voltage polarities. Here, we assumed that the soft-error mechanisms for positive and negative polarities were independent from each other, thus creating more virtual ICs. Assuming related soft-error mechanisms for different polarities and including only the more sensitive one would have resulted in only small changes to the database.

Fig. 14 illustrates the process of creating virtual IC test results as a method for including different but related results in the database. A total of 94 virtual IC test results were created for the E-field, while 115 were created for the H-field from a total of 37 real ICs. Each virtual IC test result appears as a data point in the database charts.

Most of the ICs did cause a soft error in most of the test configurations, so the corrections to the database resulting from this process were not strong. As shown in Figs. 15–18, they led to a final accumulated probability of 90%–100%.

B. Soft-Error Threshold Results

The accumulated probability results appear in Figs. 15–18. The probability of soft error is shown as a function of the peak E-field and peak H-field for the pulse used, as well as their peak time derivatives (either \( \max(\text{abs}(\frac{dE}{dt})) \) or \( \max(\text{abs}(\frac{dH}{dt})) \) ).

The field strengths were obtained using the TLP charge voltage to field strength conversion explained in the previous section. These data allow the likelihood of a soft-error problem for a given field strength to be estimated. As previously noted, the field strength can be estimated via a full-wave simulation [8] that uses a simplified geometry of the electronic system.

For example, Fig. 15 shows that among all the ICs that were disturbed in the E-field measurements, the most robust IC was disturbed at approximately 200 kV/m. Some ICs were not disturbed with the available TLP charge level; consequently, the accumulated probability did not reach 100%. The most sensitive IC was disturbed at only 6 kV/m.

The coupling of the magnetic field to the IC is caused by the loops formed by the lead frame, the bond wires and the die.
Fig. 16. Soft-error thresholds expressed as a function of the peak E-field derivative.

Fig. 17. Soft-error thresholds expressed as a function of the peak H-field.

Fig. 18. Soft-error thresholds expressed as a function of the peak H-field derivative.

Using a reasonable assumption for these loop areas and the time derivative of the disturbing magnetic field, one can estimate the induced voltages inside the IC.

To estimate the induced voltage into loops formed by the PCB ground and the internal IC structure, three different cases were considered. The small loop assumption used dimensions of $0.5 \times 0.5$ mm, which might correspond to the induction of noise voltages into the loop area formed by a bond wire. Large loops were defined as being formed diagonally across the entire IC, and they were approximately $15 \times 1$ mm. Table I shows the calculated voltage values for different loop areas.

A rate of change of 5000 A/m/ns in the magnetic field was required to disturb the very robust ICs. In accordance with the process and assumptions described previously, this leads to an induced voltage of 1.6 V for the loop, as shown in Table I. At the other extreme, the most sensitive ICs were disturbed by as little as 70 A/m/ns. The application of the large loop assumption induced a voltage of 1.3 V. These estimates do not reveal the induction process; they are only provided to illustrate the reasonable loop area assumptions that induced voltages at which soft errors began to be expected.

C. Effect of Adding a Spacer

Adding a spacer during probe calibration and IC testing should lead to approximately the same field reduction. With an added spacer, the TLP voltage would need to be increased in order to induce a soft error in an IC. Thus, adding a spacer provides a test of the quality of the database measurement methodology.

The current injected by the E-field is a function of the coupling capacitance between the probe and the sensitive area inside the IC. Ignoring fringing fields, this capacitance is inversely proportional to the distance. If a spacer is added, the field strength decreases, and the required TLP voltage increases.

For magnetic field coupling, the field does not decay very rapidly under the probe because the width of the current-carrying conductor is much greater than the distance between it and the PCB. Thus, adding a spacer should increase the needed TLP charge voltage levels, but only by a small increment as compared to the increase in the E-field levels. Other effects, such as edge effects associated with the vertical magnetic field component at the edge of the current-carrying conductor, might change more rapidly as the distance increases.

The observed average increase of the soft-error threshold in terms of field strength was 35% for the E-field and 30% for the H-field. The histogram shown in Fig. 19 reveals that the ratio of the voltage needed to create soft errors with and without spacers was nearly constant across most of the ICs.

D. Effect of Adding a 100-MHz Low-Pass Filter

Adding a low-pass filter into the TLP connection increases the pulse rise time and thus reduces the high-frequency spectral content. The basic coupling processes in the near field are proportional to the field derivative; however, multiple effects, such as low-pass filtering by LC or RC structures and the response speed of the transistors, will mitigate the effect of the field derivative. Fig. 20 demonstrates the effect of the low-pass filter on the pulse induced onto a 50-Ω loaded trace placed close to the E-field probe. The filter increased the rise time of the induced voltage from approximately 200 ps to approximately

<table>
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<tr>
<th>Magnetic field strength derivative</th>
<th>Small loop</th>
<th>Medium loop</th>
<th>Large loop</th>
</tr>
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<tbody>
<tr>
<td>70 A/m/ns</td>
<td>0.022 V</td>
<td>0.045 V</td>
<td>1.3 V</td>
</tr>
<tr>
<td>5000 A/m/ns</td>
<td>1.6 V</td>
<td>3.2 V</td>
<td>92.8 V</td>
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</table>
This study described a test methodology to determine the sensitivity of ICs toward ESD induced soft errors. The test method was applied to 37 ICs to create a novel small database showing the sensitivity of ICs typically used in consumer electronics. The developed field injection probes were able to be used for immunity testing up to approximately a few gigahertz, with a relatively constant and homogenous field above the subject IC. In most cases, the field strengths were sufficiently large to disturb most of the ICs tested. The database provides a distribution of the soft-error thresholds in terms of the field strength for the pulses used and the temporal derivative of the fields.

VI. CONCLUSION

REFERENCES


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